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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

MAIL ROOM JUL 10 1991 18 PAT. & TRADEMARK OFF.

In re application of: JOSEPH T. EVANS, JR., ET AL.

Serial No.: 582,672

Filed: September 14, 1990

Group: 233

Examiner: Alyssa H. Bowler

For: NON-VOLATILE MEMORY CIRCUIT USING FERROELECTRIC CAPACITOR STORAGE ELEMENT

RECEIVED
JUL 11 1991
GROUP 230

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

DECLARATION OF JOSEPH T. EVANS, JR.

I, Joseph T. Evans, Jr. of 13609 Verbena Place, N.E., Albuquerque, New Mexico 87112, do hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true, do hereby declare as follows:

1. I was an owner-employee of Krysalis Corporation since its founding on or about September, 1984, and was then Acting Vice President of Product Development.

...y certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on July 8, 1991
(Date of Deposit)

Roger N. Chauza, Reg. No. 29,753
Name of applicant, assignee, or Registered Representative

Roger N. Chauza
Signature

July 8, 1991
Date of Signature

2. My general responsibilities were the development of solid state nonvolatile memory devices which incorporated ferroelectric capacitors, and the management of personnel to accomplish such task.

3. Exhibit 1 is my letter dated October 20, 1986, to Mr. Dale Nixon, an attorney representing Krysalis in patent matters. In my letter of Exhibit 1, I note that there are four groups of patent disclosures, including group four, entitled: "Method of Reading Polarization of Ferroelectric Cell for Purpose of Making a Solid State Memory". Attached to Exhibit 1 is the invention disclosure material showing the several concepts and variations of the solid state memory circuits mentioned in the letter of Exhibit 1.

The invention disclosure material related to the Group 4 invention noted in pages 5-8 of Exhibit 1 includes the following subject matter:

1) ferroelectric memory cell with 1 capacitor and 1 transistor
2) 2 cells per bit architecture
3) the disturb problem and possible solutions
4) alternate architecture
5) pulsed instead of stepped read
6) dynamic sense amplifier
7) Wayne Kinney's sense amplifier scheme (Figure 17)

The different ferroelectric memory cell architectures were included in one disclosure and were considered together as it was believed that they related to the same general invention. A patent application covering both the single-transistor, single-capacitor cell architecture and the two cells per bit architecture was prepared by attorney Dale Nixon and filed in the U. S. Patent and Trademark Office.

4. Michael Cordoba was an employee of Krysalis Corporation during 1987, during which time period he was responsible for conducting numerous tests and evaluations on ferroelectric material to find a suitable ferroelectric material for fabricating nonvolatile memories.

5. Exhibit 2 is a memorandum dated March 4, 1987, that Mr. Cordoba prepared in connection with establishing a long-term fatigue (LTF) testing program for ferroelectric material developed by Krysalis. Mr. Cordoba developed a schedule, as set forth in his memo of Exhibit 2, in which fatigue structures having ferroelectric material were to be fabricated and tested at Krysalis to determine the fatigue characteristics of different types of ferroelectric compositions.

6. Exhibit 3 is a test film traveler, dated March 30, 1987. The test film traveler identifies the various wafers, 7082A-F, and the processing parameters particular to each wafer. The other pages of Exhibit B are the test results of various wafer die before actual fatigue tests were carried out. Such tests are believed to be carried out on or about March 31, 1987, and April 3, 1987, as indicated on various sheets of the test results.

7. Exhibit 4 is a document dated April 10, 1987, indicating the manner in which wafers 7096C-H and 7097A were processed at Krysalis with ferroelectric material to conduct various tests. The other papers of Exhibit C are tests of various wafer chips to accumulate parameters of the ferroelectric capacitors before undergoing fatigue tests. The wafer identified in the test report as "96C" corresponds to the wafer of the test film traveler "7096C", and so on. The test data is believed to be taken on or about April 15, 1987, the date indicated on the test printout.

8. Exhibit 5 is a report, dated April 15, 1987, which I prepared, concerning minutes of a Device Process Request Scheduling meeting. This memo sets forth the scheduling of personnel and equipment to carry out long-term fatigue tests of various types of ferroelectric material. The memo notes that until May 22, Krysalis will do one test day a week, testing up to 42 packages a day. To the best of my recollection, this was carried out.

9. Exhibit 6 is a memorandum by Michael Cordoba, dated April 24, 1987, of which I am familiar and recognize. In this memorandum and attached papers, Mr. Cordoba indicates the results of resistance measurements of top electrode (TEL) material which was deposited over the ferroelectric (FES) material. Copies of photographs dated April 27, 1987, illustrate the hysteresis loop characteristics of the capacitors on wafers 7098E and 7098F. A handwritten note on the memorandum references the photographs of the ferroelectric capacitor electrical characteristics.

10. Exhibit 7 is a memorandum dated April 28, 1987, from Michael Cordoba to myself. In this memo, Mr. Cordoba reports to me the long-term fatigue parameters of various compositions of PLZT ferroelectric materials. The various graphs attached to Exhibit 7 illustrate a change in the polarization magnitude (delta P) for various time periods shown along the horizontal axis as a logarithmic time period. The memorandum by Mr. Cordoba is self-explanatory as to the various results.

11. Exhibit 8 is a memorandum dated April 30, 1987, from Michael Cordoba to myself. According to the long-term fatigue test reported in this exhibit, Mr. Cordoba reported that Anita, a Krysalis employee, conducted tests on an 8/40/60 composition of ferroelectric material at two different frequencies (10KHZ and 1MHZ) to determine the frequency dependency of the fatigue rate of delta P. The graphical results, dated April 29, 1987, tabulate the tests conducted.

12. Exhibit 9 is a memo dated April 30, 1987, from Michael Cordoba to myself. Mr. Cordoba conducted threshold and beta tests on transistors from the process control module of a wafer vendor, and from transistors on the ECD512 wafer processed at Krysalis after covering it with a ferroelectric material. The comparative results of the threshold and beta transistor parameters are identified in the report of Exhibit 9.

13. Exhibit 10 is a memorandum from Michael Cordoba to myself, dated May 14, 1987. In this memorandum, Mr. Cordoba reports to me the results of an experiment with three different ferroelectric compositions using AC cycling to determine the extent of fatigue degradation of the material. Various graphical results of the tests are attached to the exhibit.

14. Exhibit 11 is a memorandum from Michael Cordoba to myself, dated May 19, 1987. The fourteen graphs attached to the exhibit illustrate the various capacitor parameters as a function of log time, and as a function of different types of ferroelectric material being tested. The memo states that certain tests were carried out for 678.1 hours of ferroelectric capacitor operation. The memo by Mr. Cordoba is self-explanatory as to the ferroelectric material tests.

15. Exhibit 12 is a memorandum by Michael Cordoba to myself, dated May 21, 1987. The various test printouts attached to the exhibit identify the ferroelectric parameters resulting from the tests conducted on May 19, 1987, and as reported in the memo of Exhibit K. Mr. Cordoba proposes additional tests which can be conducted using different numbers of ferroelectric layers and buffer layers of material.

16. Exhibit 13 is a memorandum from Michael Cordoba to myself, dated June 2, 1987. This memorandum by Mr. Cordoba identifies the results of tests on ferroelectric capacitors prepared on ECD512a CMOS wafers, and on non-CMOS wafers. Various tests were conducted on May 26, 1987, and June 2, 1987, the results of which are attached to Exhibit 13.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: 7/3/91

Joseph T. Evans, Jr.

B-23727

(1)

Attn: Dale Nixon
Richards, Harris, Medlock & Andrews
2900 One Main Place
Dallas, Texas 75250

October 20, 1986

Dear Dale,

Enclosed, you will find the following patent disclosures from Krysalis Corporation:

1. Method for preparing PLZT and PZT sol-gels and fabricating ferroelectric thin films.
2. Method for patterning PLZT thin films
3. Ferroelectric Capacitor Structure
4. Method of reading polarization of ferroelectric cell for purpose of making a solid state memory.

These submissions represent the state of the art of our technology, and probably that of the rest of the world, in fabricating a ferroelectric, solid state memory based on perovskite ferroelectrics. The disclosures cover most of the building blocks required to make a memory device. There may actually be more than four patents and groups of claims in these submissions. For instance, #4 represents IC circuitry concepts for making a solid state memory and there are several concepts and variations mentioned in the disclosure.

The technology represented in the submissions is different than that in our original patent application of June, 1985. We may want to start our technology patents using these as the umbrella. However, it may be of use to use that original application as the umbrella. (We have serious doubts about the viability of the original patent as it is written!) Please review these disclosures and work out a framework for the patent applications. When you are ready, please visit us here in Albuquerque and we will finalize our strategy as well as let you speak with the inventors to fill in any gaps that exist.

Be aware that we have quite a few disclosures in the works based on our technology now that we are fairly confident of our capabilities. Examples of things to come are actual memory architectures, a non-volatile latch similar to an SRAM, process improvements, and actual ASIC products. A subject we must discuss is the workload involved in processing these applications, the number of people on your staff needed, and the cost to us. Please contact us when you are ready to visit Krysalis in Albuquerque.

RECEIVED
OCT 21 1986
Richards, Harris, Medlock & Andrews

Sincerely,

Joseph T. Evans, Jr.

Joseph T. Evans, Jr.
President

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4200 Osuna N.E. Suite 102, Box 106
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KRYSALIS CORPORATION CONFIDENTIAL

Krysalis Corporation
Patent Disclosure
Subject: Method of reading polarization of ferroelectric cell for purpose of making solid state memory.
Date: October 18, 1986
By: Richard Womack, Joe Evans, Wayne Kinney, William Miller

<u>Description of Invention</u>

Disclosed is a method, and variations thereof, of reading the polarization of a ferroelectric capacitor. Since the zero voltage, remnant polarization state of a ferroelectric capacitor, unlike a linear capacitor, can have a non-zero value, a ferroelectric capacitor can be used to make a solid state memory requiring no moving parts.

The basic invention consists of the ferroelectric cell, C_{fe}, in series with a digital switch, Sw_1, such as a bipolar or MOS transistor, and then in series with a capacitor, refered to as the sense capacitor, C_s.

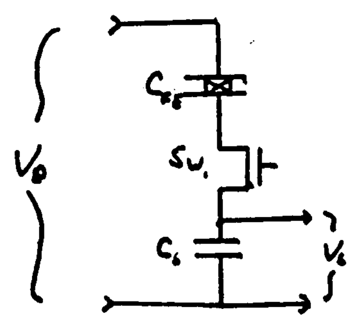


Figure A

When a voltage is applied across the series components, Sw_1 prevents any charge transfer to take place until it is turned on and represents a method of addressing a particular component in an array of components. Parasitic losses must be taken into account in actual designs to prevent leakage of charge when the device is not selected. The polarization state of the ferroelectric capacitor after drive voltage, V_d, application will consist of non-remnant charge, P_{nr}, resembling that of a linear capacitor, plus whatever zero voltage remnant charge, P_r, is present in the ferroelectric capacitor before V_d is applied. Polarization, P, is defined as charge/unit area, usually square centimeters. As a consequence of charge conservation, with the digital switch on C_s will take on the same

polarization state as the ferroelectric capacitor. The voltage, V_s, across C_s will follow the well known capacitor equation:

$$V_s = \frac{Q}{C_s} \qquad \text{Eq 1}$$

Q = Charge driven out of C_{fe}

In C_{fe}, Q consists of

$$Q = (P_r + P_{nr})A_{fe} \qquad \text{Eq 2}$$

A_{fe} = Area of C_{fe}

thus,

$$V_s = \frac{(P_r + P_{nr})A_{fe}}{C_s} \qquad \text{Eq 3}$$

and

$$V_s = \frac{P_r A_{fe}}{C_s} + \frac{P_{nr} A_{fe}}{C_s} \qquad \text{Eq 4}$$

The non-remnant term will be present anytime a voltage is applied. The remnant term is the data retained term. If the P_r state before application is the result of a voltage applied in the same direction as V_d for the read, then the remnant term will be very small. If the opposite voltage is used to write P_r before the read, the remnant term will be large. Thus, in the circuit described previously, the V_s for reading polarization of the ferroelectric cell has the following mathematical description:

$$V_s(V_d) = \text{Remnant Voltage}(V_d) + \text{Common Mode Voltage}(V_d) \quad \text{Eq 5}$$

If V_d is returned to 0 volts after application but before reading V_s, the Common Mode Voltage will also return to 0 volts, subject to discharge rules, while the Remnant Voltage will remain across C_s.

The read method described herein is destructive of the information held within the cell. The data must be rewritten into the cell after the read is complete.

What follows are variations of the method when applied to solid state microelectronics circuits.

FERROELECTRIC MEMORY CELL CONFIGURATIONS

1) Ferroelectric Memory Cell with 1 Capacitor and 1 Transistor

Ferroelectric (FES) capacitors have the property that if the voltage across the capacitor changes from (Figure 2) Vcell = 0 at P = P0 to Vcell = +VD, the amount of charge that has been moved across the capacitor is given by (Ps - P0) Area. Thus, if the capacitor was polarized to P1 the charge moved would be given by (Ps - P1)Area. Therefore, the difference in charge between a stored "1" and a stored "0" would be
(Ps -P0)A - (Ps - P1)A = (P1 -P0)A.

One method of detecting this charge difference would be to charge a capacitor Cs (Figure 3) with it, causing a change in voltage Vs and then sensing the voltage change. This sense capacitor could, in addition to standard semiconductor capacitances (SiO2, P-N junction etc.), be made out of FES such that the ratio of the cell capacitor and the sense capacitor would track over processing and temperature.

Assuming an N-channel MOS transistor, WL1 and WL2 (Figure 3) are normally low to hold transistors M1 and M2 "off" when unaddressed. Capacitors C1 and C2 have been "polarized" to either P1 or P0. P1 and P0 represent data storage. A typical timing sequence for reading the data stored in C1 is shown in Figure 4. It is important that node V1 is precharged to the same voltage as DL1 because 0 volts are desired across the FES capacitors while they are not addressed so that when they are addressed they start out at P0 or P1. It is also important that V1 is precharged to the same voltage that the substrate is biased, because the junction leakage on the node would gradually discharge the node to the substrate level or 1 VT below WL1 (whichever is higher) if the cell were not addressed for long periods of time. This would cause a voltage to develope across the capacitor C1 and potentially disturb the data that had been written into the cell i.e. a "0" would go to a "1". This would not be as large a problem if the cell were cycled frequently. One of the major problems with a cell configuration of this sort is developing a reference voltage that tracks A(P1 - P0)Cs over processing, temperature and fatigue of the cell capacitor.

2) 2 Cells per Bit Architecture

Shown in Figure 5 this architecture doubles the signal size and provides reference signal from a cell with the same processing and temperature characteristics. The number of cycles of the 2 cells of each bit is also the same. The fatigue characteristics should track to some extent also.

Two timing sequences for this arrangement are shown in Figures 6a and 6b assuming a 1 written into the bit. Figure 6a is very similar to Figure 4 with the exception of being applied to a 2 cell bit. In this scheme DL1 and DL2 behave exactly the same and thus can be tied together. This shorting could be taken advantage of in the layout and result in less area per bit than the Figure 6b scheme. The timing scheme in Figure 6b accomplishes the restore of the 1 and 0 simultaneously and could result in a faster read/restore cycle time.

3) The Disturb Problem and Possible Solutions

Figure 7 shows the parasitic junction diodes on the drains of the transistor. The diode on node V1 to substrate represents a parasitic capacitance to substrate also. When DL switches from low to hi, node V1 capacitively couples hi. If the cell is unaddressed i.e. WL is low, the amount of voltage dropped across C1 is dependent on the capacitance divider between C1 and DS1. C1, being a ferroelectric capacitor with a high dielectric constant, can have a value many times that of DS1, but a small delta V can develope across C1. This delta V is proportional to the swing on DL and dependent on the capacitance ratio.

As shown in Figure 10, if the capacitor is polarized to PO and a small positive delta v is applied and then Vcell is taken back to 0 volts, some polarization may be lost. This assumes that there is no threshold voltage that below which there is no polarization loss or that delta v is greater than the threshold. If a small amount of polarization is lost every cycle, then the total or at least half of the polarization is lost.

Figure 8 shows a circuit that may help. M2 is turned "on" when the cell is unaddressed. M2 effectively decreases the impedance of C1 during the disturb pulse such that delta V is decreased also. M2 however, is not as effective at high slew rates on DL and also requires another signal to be generated (WLX).

Figure 9 shows another solution where the capacitor C1 is isolated from DL while the cell is not addressed. Also, nodes V1 and V2 look very similar as far as parasitics to substrate are concerned. Thus, noise from substrate would have a tendency to be more common mode for this case. The circuit in Figure 9 would decrease the delta V by several orders of magnitude compared to Figure 7. The disadvantage here (as in Figure 8) is the addition of another transistor per cell. Figures 8 and 9 can also be used in the 2 cells per bit architecture.

4) Alternate Architecture

Figure 11 shows an alternate 2 cells per bit architecture (can also be used in 1 cell per bit scheme). In this scheme DL1 is parallel to WL1 instead of being parallel to BL1. What this implies is that DL1 only switches when WL1 is addressed and thus decreases the disturb problem mentioned earlier when DL1 switched (Figure 5) and WL1 did not i.e. the DLs only go to cells that are addressed simultaneously and do not disturb those that are not addressed. This scheme is not as good as that shown in Figure 9 from a disturb standpoint because DL1 and V1 do not have similar substrate, or layout characteristics and thus is more likely to have a difference voltage develope across C1 due to noise. The swing on DL1 (when unaddressed) should be at least an order of magnitude less than in the Figure 5 scheme i.e. noise swing compared to the signal swing on DL1 should be at least an order of magnitude less, and thus the delta V developed should be that much less. The scheme of Figure 11 has the advantages over Figure 8 and 9 is that it does not require extra transistors or

signals. The Figure 11 scheme is also superior to the Figure 9 scheme in switching characteristics because it has less impedance in the DL1 path and less capacitance on WL1. A possible timing sequence is shown in Figure 12. This figure assumes a 1 is written into the cell. This sequence is very similar to that in Figure 6a.

5) Pulsed Instead of Stepped Read

If a capacitor polarized to P1 at Vcell = 0v is taken to Vcell = +VD, and then taken back to Vcell = 0v, it should eventually return to P1. If a capacitor polarized to P0 is taken to Vcell= +VD and then back to Vcell = 0v, it should then have polarization P1. The change in polarization in this case is P1 - P0. This is the same as the charge differential when both cases were just taken to Vcell = +VD. Furthermore, if a capacitor polarized at P1 is taken to any positive voltage and then returned to Vcell = 0v, the polarization should return to P1. Thus a capacitor in a P1 state does not need full VD drive to be restored. The timing in Figure 12 can become that in Figure 14. This timing sequence has the advantage that if the P vs Vcell curve of C1 and C2 did not track with fatigue, then the differential signal would not be affected, because the capacitor at P1 would cancel himself out and the capacitor at P0 would determine the differential signal to be sensed. The disadvantage is that one has to wait for DL1 to switch twice before beginning to sense. The timing scheme in Figure 14 also lends itself to using one cell per bit because the resulting signal out from P1 or P0 polarization is referenced to ground i.e. P1 polarization would lead to 0 or some small voltage Vs1 and P0 would lead to an absolute voltage of A(P1 -P0)Cs for that capacitor. Wayne Kinney suggested the Figure 14 timing sequence.

Because there is a capacitor divider in the actual circuit between the cell capacitor and Cs, not all the drive voltage may be across the cell capacitor during the read and thus not all of P0 polarization may lead to differential signal. This case is shown in Figure 13 such that the voltage across the capacitor goes to Vr and then back to Vcell = 0v. The polarization in this case goes to P1' and the signal to be sensed is approximately A(P1' - P0)Cs. The voltage Vr is determined by the ratio of the cell capacitance (say C1) to Cs i.e.

Vr = CsVD/(C1 + Cs).

6) Dynamic Sense Amplifier

Because the charge dumping causes a destructive read, a restore operation is required. This is very analogous to a DRAM operation. The voltage magnitudes could be on the same order also. The destructive read implies synchronous operation. Therefore, a dynamic differential sense amp employing similar techniques used in DRAMS may be used. Such a sense amp is shown in Figure 15. Figure 16 shows the revised timing of Figure 14 with the additional signals.

7) Wayne Kinney's Sense Amplifier Scheme (Figure 17)

The idea is to maximize the voltage drop across the cell capacitor by integrating the charge using an inverting amplifier with capacitance feedback. The hope is that the voltage on BL would remain constant and the total charge on DL would be across the cell capacitance and thus avoiding the loss of signal shown in Figure 13 with the capacitance divider method. The trade offs here involve the design complexity of the inverting amplifier, its speed, offset, and common mode range. If a very linear amplifier with low standby current, low offset and a common mode range encompassing the BL precharge voltage, can be designed, the a superior sense amp would result in allowing use with a smaller input signal.

Because of the complexity of the circuitry, it is unlikely that op amp sensing circuits would find acceptance in high density digital memories. However, this sensing scheme would be useful in arrayed analog memory schemes where analog data is stored and sensed ~~in~~ as continuous values and not discrete binary values. An op amp with a capacitor in the feedback loop can be the first stage of a sample / Hold / Analog to Digital converter circuit to digitize analog values stored in ferroelectric cells.

JJL

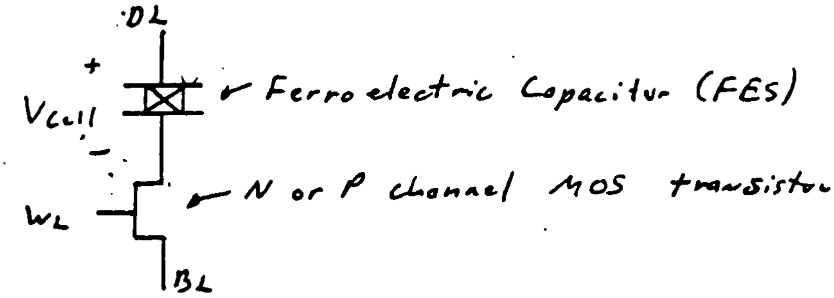
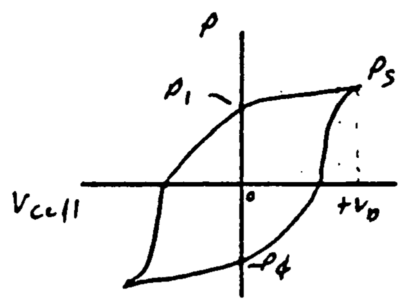


Figure 1



$$P = \frac{Q}{A} = \frac{\text{Charge}}{\text{Area}}$$

Figure 2

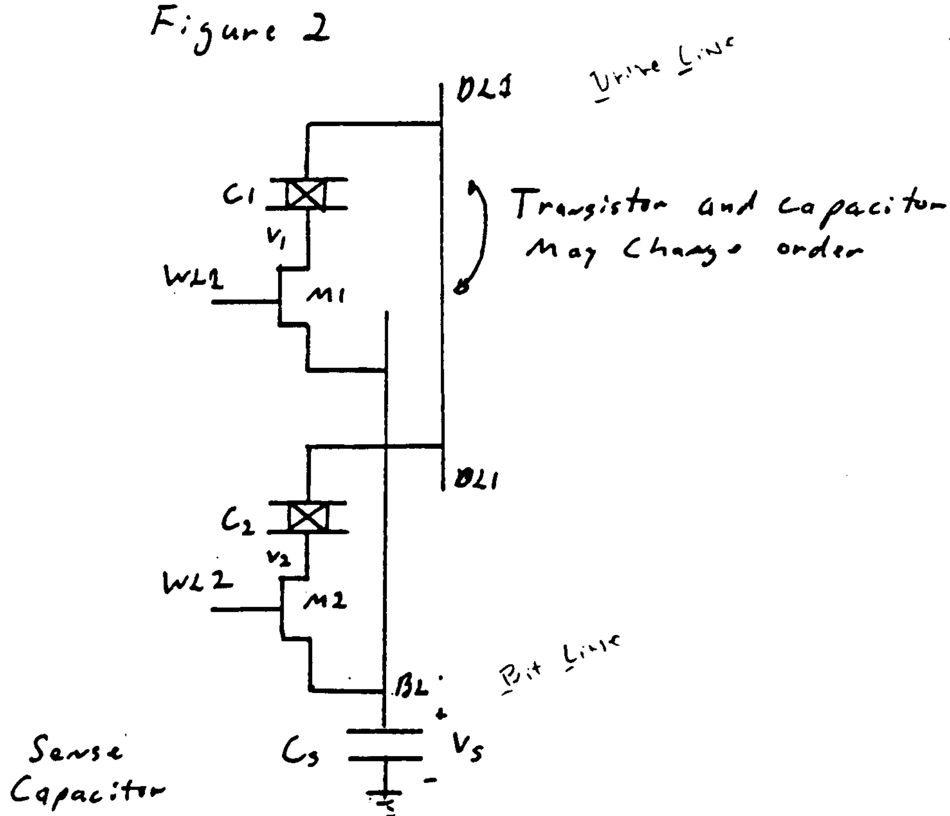


Figure 3

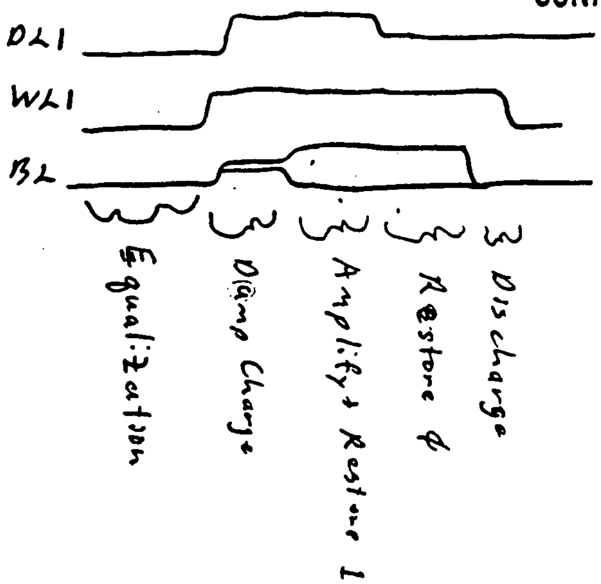


Figure 4

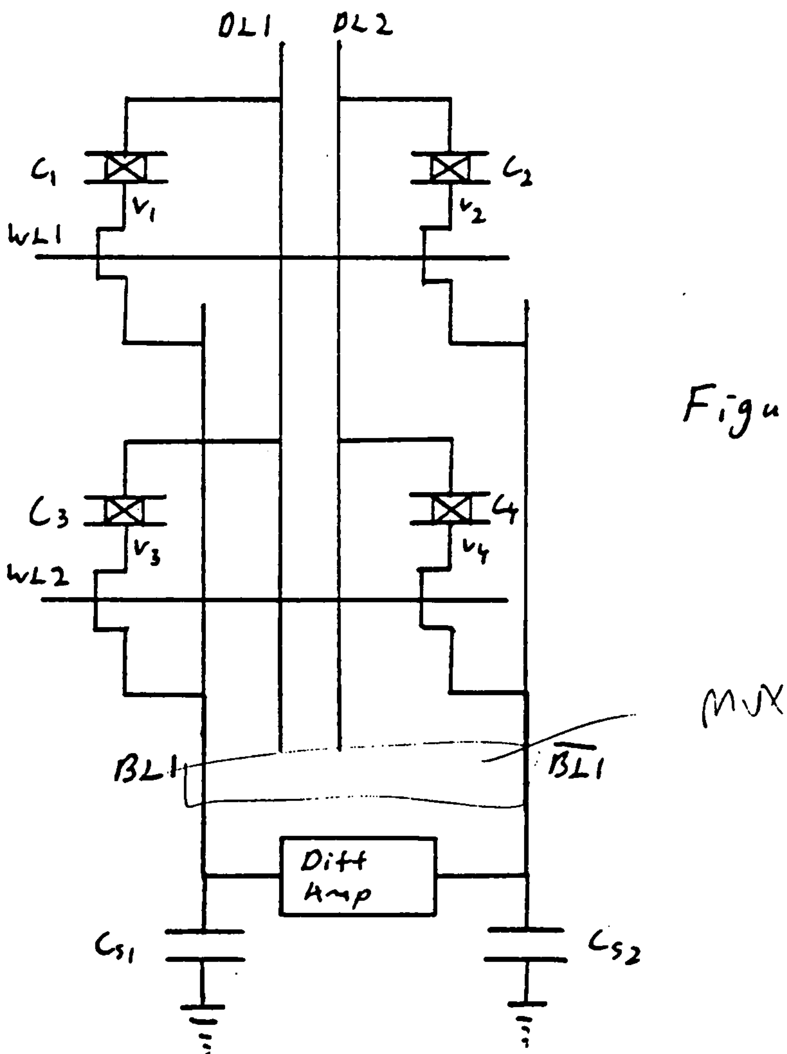


Figure 5

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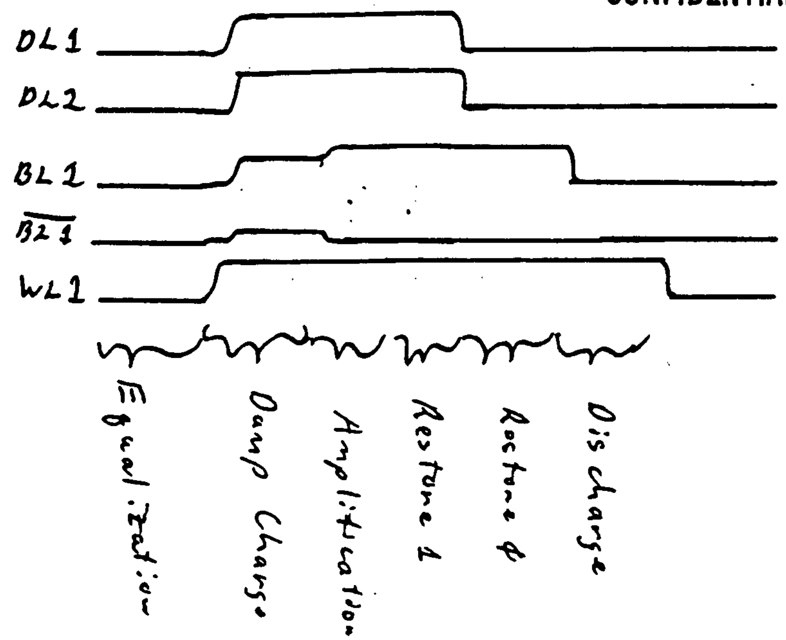

Figure 6a.

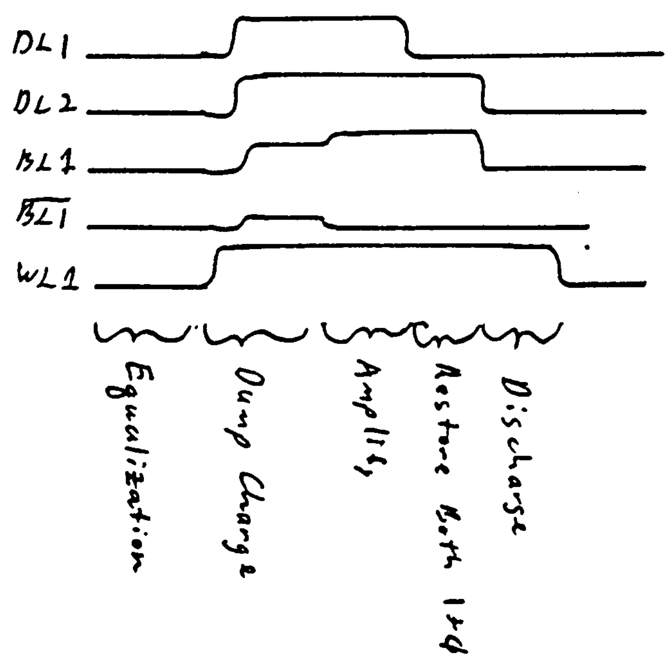

Figure 6b.

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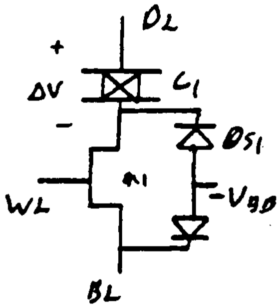

Figure 7

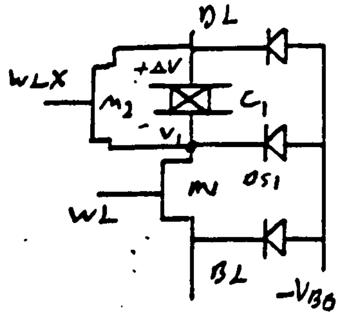

Figure 8

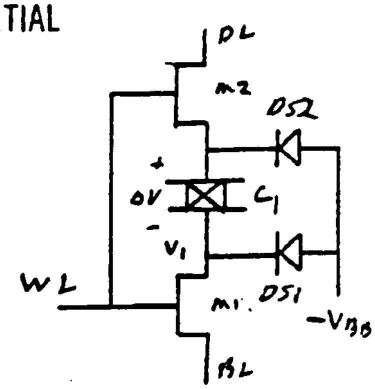

Figure 9

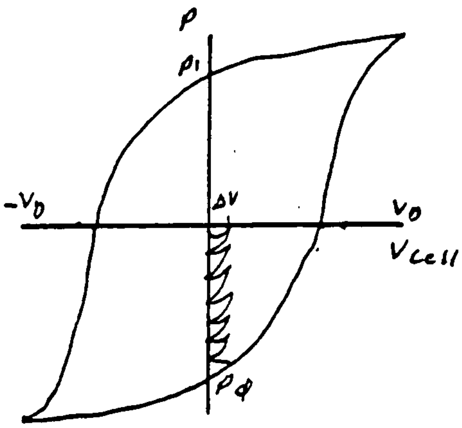

Figure 10

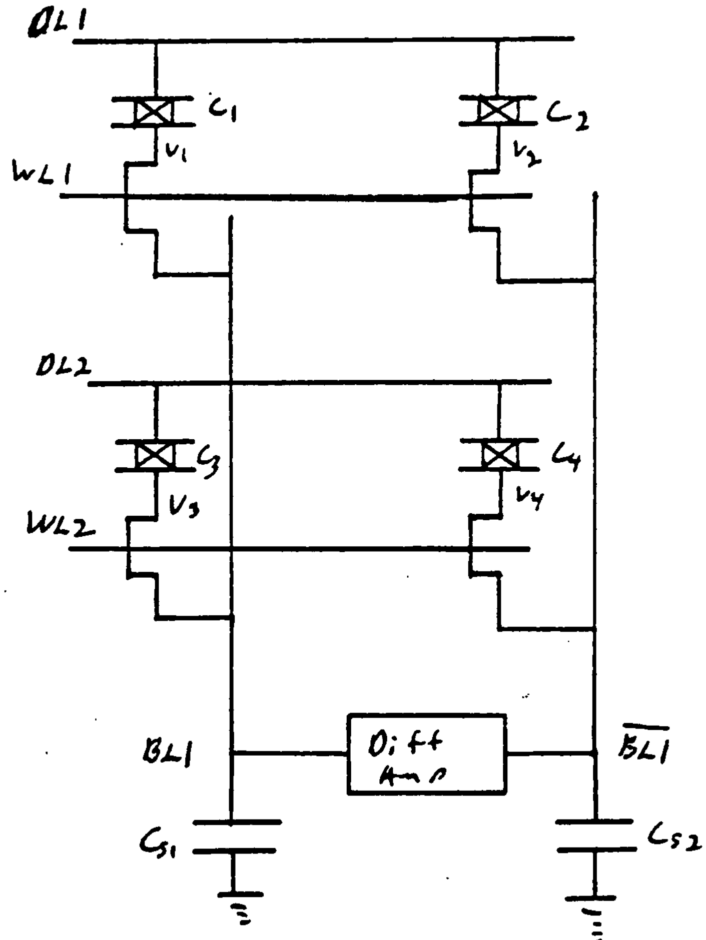

Figure 11

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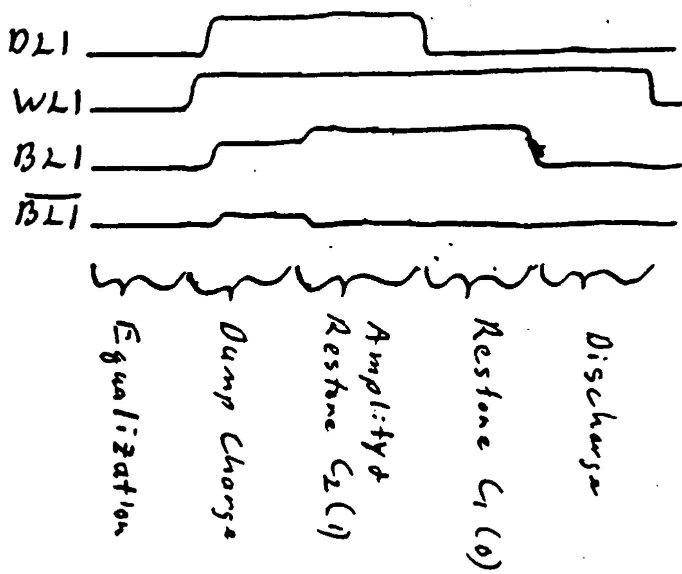

Figure 12

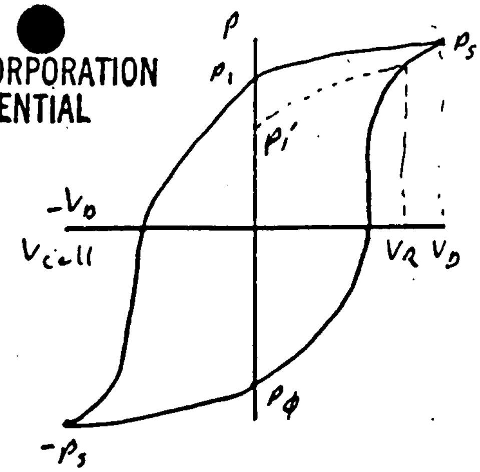

Figure 13

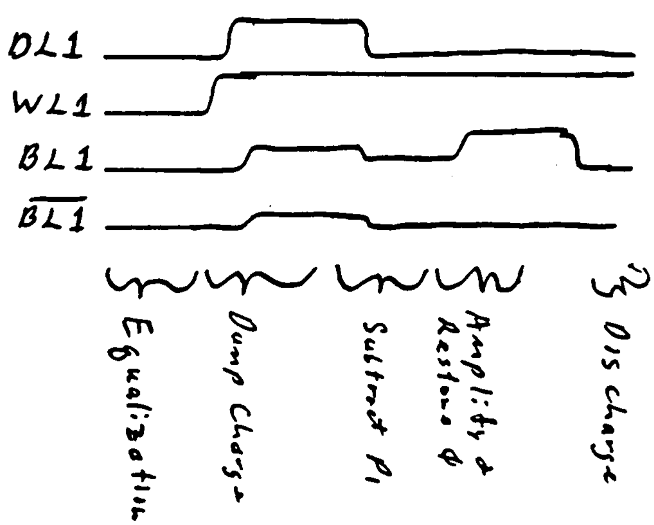

Figure 14

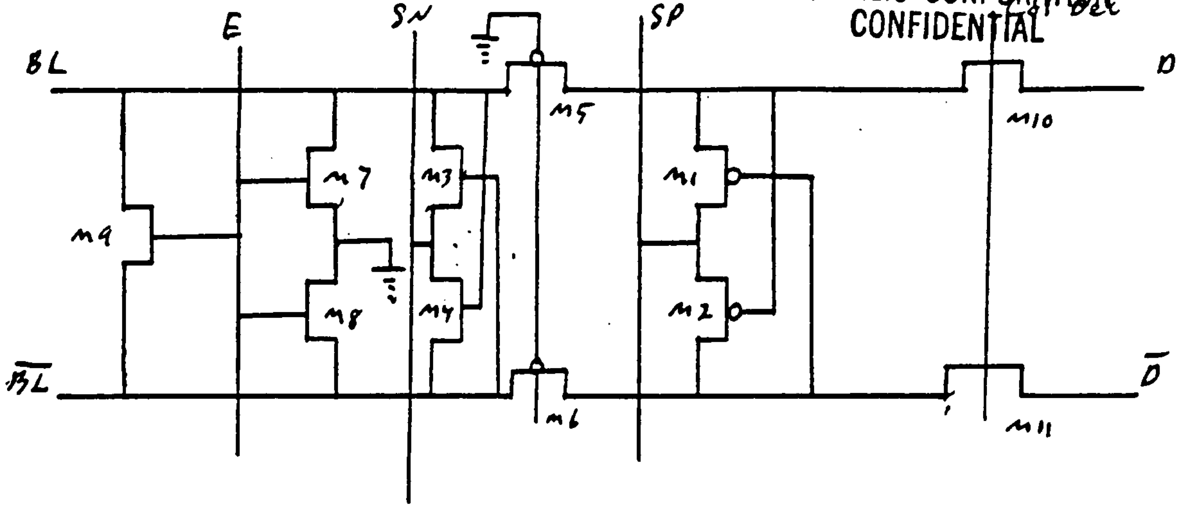

Figure 15

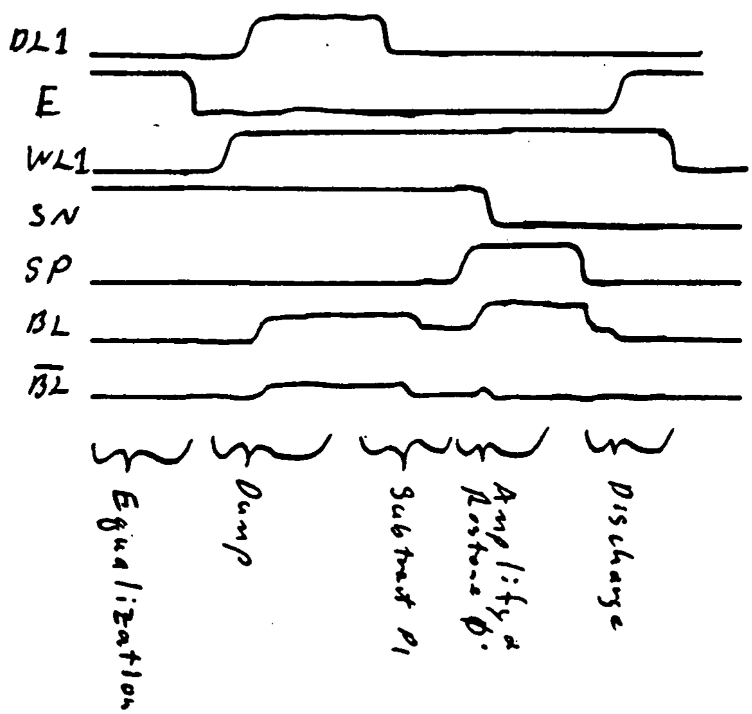

Figure 16
(For Fig 15)

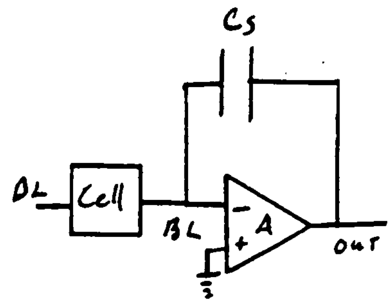

Figure 17

Problems Solved

Until now, all viable memories using electric field only to store data have consisted of silicon based devices fabricated using microelectronic techniques. However, only silicon nitride has an intrinsic non-linear memory effect similar to ferroelectric materials that can be used to make non-volatile memories. Silicon nitride memories, otherwise known as MNOS devices, have proven to be notoriously unreliable and exhibit a wearout mechanism. Another method of non-volatile memory in silicon has used electron tunneling in the presence of high electric fields to trap charge on a MOSFET gate. This technique, commonly called Electrically Eraseable Programmable Read Only Memory, also exhibits a wearout phenomenon.

Recent advances in ferroelectric thin film technology and machining have created the potential for building ferroelectric capacitors with remnant polarization onto silicon wafers. Using the above described invention, non-volatile memories with long term or nearly infinite retention, high densities, low voltages, high speeds, and unlimited reads and writes may be fabricated at a reasonable cost. The availability of fast, cheap, non-volatile, solid state memories will allow the design and fabrication of electronic computers and systems heretofore unheard of.

What was done. When.

January, 1985 - Basic solid state memory mechanism demonstrated on bulk ferroelectric material by Joe Evans.

November, 1985 - Ferroelectric thin films demonstrated by Joe Evans and William Miller.

January, 1986 - Invention concept demonstrated on thin ferroelectric film capacitors using XT computer as controller.

September, 1986 - Zero fatigue effect demonstrated on ferroelectric thin films capacitors by Joe Evans and Wayne Kinney. Lack of fatigue effect makes destructive readout viable for commercial applications.

September, 1986 - Architectural design for nonvolatile memory incorporating invention is completed by Richard Womack, Krysalis Corporation with assistance from Joe Evans, Wayne Kinney, and William Miller.

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KRYSALIS CONFIDENTIAL

TO: Distribution Date: 03-04-87

FROM: Michael Cordoba

SUBJECT: Minutes LTF System (LTF1.TXT)

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The following is my view of the LTF system and the schedule for bringing parts of the system online. My philosophy for the schedule (which I believe was also the general consensus of those in the meeting) is that we need to start collecting room temperature first and I MUST put in place what is necessary to do this. I will put effort, into getting other temperature boards up - but primary emphasis will be to get room temperature up and running by the end of this month. My feeling is that we need to start collecting data soon and we should do what is simple first, and then get complicated.

Schedule for First Board:

- Receive masks March 5 or 6. ✓
- Finish processing wafers March 10. → March 20
  The following compositions were agreed to of 4 wafers each:
  8/40/60
  3/40/60
  0/50/50
  15/0/100
- Packages to be received by March 11. ✓
- Wafers and packages to be sent to Indy Electronics March 12. → March 24
- Packaged parts to be received March 30. → April 3 ?
- Room Temp LTF to go online by March 31. → April 6
  The 5 columns will be organized in the following manner.
  4 chips of 8/40/60 Structure 1(i.e. 100 X 100)
  4 chips of 3/40/60 " " " " "
  4 chips of 0/50/50 " " " " "
  4 chips of 15/0/100 " " " " "
  3 chips of 8/40/60 " 1A(i.e. 100X 100 w/ Al)

[illegible]
[illegible] cleaned
[illegible] High Temp
✓ [illegible] High Temp
✓ test bd built
✓ Packages sent out LTF
✓ technician hired
(starts 3/30 Mon)
(E1 metal mask
LF ordered)

Technique for bonding?

The 5 columns will be pulsed in the following manner.
- The first 2 columns will be pulsed with a continuous pulses (either Sine or Square) from -8 to 8 volts.
- Column 3 will be pulsed with a square wave from 0 to 8 volts.
- Column 4 will be DC stressed at 8 volts.
- Column 5 will have the three state pulse of 8,0 and -8 volts.

In conjunction with this happening I need to prepare the following within a month ... BEFORE LTF SYSTEM COMES ONLINE. I think it is imperative that I do items 1 and 2 below.

Rxn w/ Pt-Al or other. happens at 450°C

However, I feel that I can let other items fall behind slightly so that 1 and 2 can be finished - so that LTF System can be used at room temperature.

** 1. Design a board to measure polarization of the capacitors placed in LTF.

** 2. Learn enough ASYST that I can write a program to collect the data.

3. Design and checkout board to do 3 state pulsing.
4. Order material for 3 other boards.
    - boards
    - oven
    - packages
    - zips
    - resistor networks.
5. Bring Bonder online.
6. Select low temp and high temp ovens.
7. Order a frame or a support for the boards.
8. Hire a technician.

TEST FILM TRAVELER Krysalis Confidential March 30, 1987

FILM ID	SUBSTRATE	BEL	GEL ID	CTS	TEL	BAKE	ANNEAL
7082A	Orbit TW	B58-4	G7055	8	55	2@400	30 @ 650°C / O_2
NOTES: NITRIDE SUBSTRATE, ANNEALED AT 750°C O_2 BEFORE BEL.							
7082B	Orbit TW	B64-1	G7055	8	"	2@400	"
NOTES: TiO_2 ON ~~NITRIDE~~ NITRIDE SUBSTRATE, ANNEAL 750°C O_2 BEFORE BEL							
7082D	Orbit TW	B64-2	G7055	8	"	2@400	"
NOTES: OXIDE SURFACE, NITRIDE REMOVED.							
7082E	Orbit TW	B64-3	G7055	8	"	2@400	"
NOTES: NITRIDE, 750°C ANNEAL O_2							
7082F	Orbit TW	B64-4	G7055	8	"	2@400	"
NOTES: NITRIDE, NO ANNEAL.							

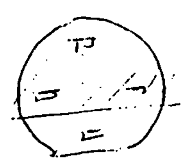
* ADDITIONAL NOTES

7082 A - BLISTERED, TESTABLE IN SMALL AREA ONLY

— O.K.

7082 B } .. O.K. TESTABLE ALL OVER
7082 D }

7082 E } FAIR TESTABLE
7082 F }



— O.K.

* PURPOSE OF TEST. SUBSTRATE CAN AFFECT $\Delta \rho$ ON LCDM'S. WE HAVE NEVER CONFIRMED WHAT OCCURS ON TDC1. IMPORTANT OBSERVATIONS RELATIVE TO IMPROVING FET CHARACTERISTICS.

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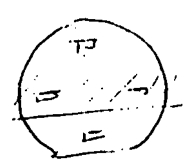

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Tested values BEFORE fatigue: 01/01/80 page 1 Tested 3/31

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82B	.	*******	.012	.952	.000	9.04E -12	.24
82B	163.	.0174	3.016	.830	.840	2.17E -11	14.74
82B	.	*******	-.149	*****	.000	8.94E -12	.13
82B	1.	*******	-.169	*****	.000	9.18E -12	.13

Tested values BEFORE fatigue: 01/01/80   page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Rat1	Vc	log(I)	Ps-Pr
82B	.	*******	.114	.121	.000	9.41E -12	.02
82B	147.	.0183	2.420	.850	.933	1.87E -11	13.67
82B	.	*******	-.008	3.000	.000	8.79E -12	.01
82B	1.	*******	.000	1.000	.000	8.88E -12	.33

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82B	.	*******	.000	1.000	.000	8.86E -12	.04
82B	169.	.0185	2.839	.841	.867	1.99E -11	15.06
82B	.	*******	.227	*****	.000	8.44E -12	-.14
82B	1.	*******	-.129	2.179	.000	8.31E -12	.24

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82B	.	*******	.024	.846	.000	8.98E -12	.13
82B	161.	.0185	3.039	.826	.867	1.90E -11	14.43
82B	.	*******	.000	1.000	.000	8.54E -12	.02
82B	1.	*******	-.208	-.710	.000	8.56E -12	.09

ted values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82B	.	*******	-.196	-.724	.000	8.88E -12	.08
82B	165.	.0183	2.980	.834	.880	1.77E -11	14.94
82B	.	*******	.145	.119	.000	8.26E -12	.02
82B	1.	*******	-.012	1.042	.000	8.23E -12	.29

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82D	.	*******	.024	.905	.000	8.82E -12	.22
82D	111.	.1068	-.192	-.361	.907	2.31E -11	.05
82D	.	*******	.043	.784	.000	7.91E -12	.16
82D	1.	*******	-.051	2.182	.000	8.08E -12	.09

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82D	.	*******	-.114	2.706	.000	8.75E -12	.18
82D	147.	.0678	2.706	.844	.827	1.94E -11	14.67
82D	.	*******	.102	.278	.000	8.77E -12	.04
82D	1.	*******	-.251	*****	.000	8.42E -12	.14

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82D	.	*******	-.165	*****	.000	8.37E -12	.09
82D	161.	.0184	2.980	.832	.933	1.82E -11	14.75
82D	.	*******	.271	*****	.000	7.52E -12	-.20
82D	1.	*******	.012	.500	.000	7.13E -12	.01

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82D	.	*******	-.016	-.333	.000	8.13E -12	.00
82D	.	*******	[illegible]	.851	.000	7.67E -12	.22
82D	.	*******	.208	*****	.000	7.43E -12	-.20
82D	1.	*******	.004	.952	.000	7.49E -12	.08

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82D	.	*******	.224	*****	.000	8.75E -12	-.15
82D	160.	.0182	3.188	.821	.907	1.77E -11	14.62
82D	.	*******	.188	*****	.000	7.29E -12	-.09
82D	1.	*******	.255	-.857	.000	6.81E -12	-.12

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82D	.	*******	.165	-.167	.000	1.12E -11	-.02
82D	173.	.0175	2.682	.853	.733	1.88E -11	15.61
82D	.	*******	.024	2.500	.000	7.47E -12	-.04
82D	1.	*******	-.086	-.222	.000	7.30E -12	.02

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82E	.	*******	-.125	-.778	.000	8.55E -12	.05
82E	18.	-.3066	3.749	.651	1.333	2.70E -11	7.00
82E	.	*******	.110	.000	.000	7.74E -12	.00
82E	1.	*******	.212	-.421	.000	8.29E -12	-.06

ted values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82E	.	*******	.102	-.083	.000	8.55E -12	-.01
82E	1.	*******	.275	*****	1.240	3.68E -11	-.20
82E	.	*******	.204	-.625	.000	8.07E -12	-.08
82E	1.	*******	.086	.542	.000	7.89E -12	.10

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82E	.	*******	.102	.316	.000	7.56E -12	.05
82E	115.	.0176	2.565	.809	.680	2.14E -11	10.83
82E	.	*******	-.039	1.833	.000	8.04E -12	.09
82E	1.	*******	.165	.364	.000	8.15E -12	.09

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82E		*******	.110	-.556	.000	8.13E -12	-.04

82E	1.	*******	.180	-.211	.000	8.21E -12	-.03

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82E	.	*******	.157	-.111	.000	8.37E -12	-.02
82E	147.	.0182	3.365	.803	.720	2.58E -11	13.68
82E	.	*******	.055	.774	.000	8.17E -12	.19
82E	1.	*******	.267	-.062	.000	7.82E -12	-.02

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82E	.	*******	.157	*****	.000	8.26E -12	-.08
82E	146.	.0183	2.714	.835	.653	2.52E -11	13.71
82E	.	*******	-.094	1.500	.000	7.06E -12	.28
82E	1.	*******	.078	.286	.000	8.30E -12	.03

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82F	.	*******	.118	-.667	.000	8.51E -12	-.05
82F	145.	.0191	2.753	.831	.800	2.06E -11	13.52
82F	.	*******	-.047	.500	.000	8.04E -12	-.05
82F	1.	*******	-.196	*****	.000	8.16E -12	.18

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82F	.	*******	.118	-.500	.000	1.09E -11	-.04
82F	156.	.0189	3.239	.818	.960	1.44E -11	14.56
82F	.	*******	.157	.167	.000	8.10E -12	.03
82F	1.	*******	-.173	1.917	.000	8.21E -12	.36

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82F	.	*******	.102	-.083	.000	8.55E -12	-.01
82F	1.	*******	.275	*****	1.240	3.68E -11	-.20
82F	.	*******	.204	-.625	.000	8.07E -12	-.08
82F	1.	*******	.086	.542	.000	7.89E -12	.10

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	(E-12)	tan(del)	uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82F	.	*******	.000	1.000	.000	9.83E -12	-.01
82F	166.	.0189	3.514	.820	.880	2.05E -11	16.05
82F	.	*******	.220	*****	.000	8.95E -12	-.13
82F	1.	*******	-.235	*****	.000	7.98E -12	.25

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82F	.	*******	.196	*****	.000	8.51E -12	-.10
82F	167.	.0189	2.580	.856	.920	1.93E -11	15.37
82F	.	*******	.133	*****	.000	9.50E -12	-.10
82F	1.	*******	-.016	1.400	.000	9.34E -12	.05

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82F	.	*******	.141	-.286	.000	8.68E -12	-.03
82F	165.	.0194	3.059	.835	.947	1.95E -11	15.46
82F	.	*******	.055	.759	.000	9.14E -12	.17
82F	1.	*******	.039	.500	.000	9.15E -12	.04

cell/vers.	WAFER	Struc./Area	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	75B		183.	.0217	4.333	.805	1.360	2.58E -11	17.91
1.P2	75B	1-1	188.	.0288	4.047	.813	1.480	2.25E -11	17.56
	75B		182.	.1626	4.169	.809	1.467	2.45E -11	17.66
	75B		53.	1.3317	3.988	.816	1.333	2.30E -11	17.69

Tested values BEFORE fatigue: 01/01/80 page 1

	WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	75B		180.	.0163	5.110	.776	1.013	2.64E -11	17.75
	75B		186.	.0187	4.549	.796	1.000	2.27E -11	17.71
2.P1	75B	1A-1	186.	.0187	4.714	.788	1.120	2.31E -11	17.54
	75B		190.	.0187	3.490	.830	.973	1.91E -11	17.05

Tested values BEFORE fatigue: 01/01/80 page 1

	WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	75B		179.	.0158	4.600	.792	1.027	5.06E -11	17.53
	75B		184.	.0122	4.443	.799	.987	2.77E -10	17.67
1.P3	75B	1-2	66.	-.0774	4.435	.798	.987	4.10E -11	17.56
	75B		188.	.0180	3.478	.830	.973	3.04E -9	17.02

Tested values BEFORE fatigue: 01/01/80 page 1

	WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
see retest	75B		.	*******	.020	.821	.000	9.06E -11	.09
next page.	75B		.	*******	.086	-.375	.000	1.09E -11	-.02
2.P2	75B	1A-2	.	*******	-.153	*****	.000	1.06E -11	.13
	75B		1.	*******	-.035	5.499	.000	9.71E -12	.04

Tested values BEFORE fatigue: 01/02/80 page 1

	WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	75B		181.	.0151	4.310	.803	1.000	2.64E -11	17.57
	75B		188.	.0184	3.604	.829	.973	2.05E -11	17.41
1.P4	75B	1-3	188.	.0182	3.859	.819	1.040	2.10E -11	17.43
	75B		190.	.0182	3.439	.835	.893	2.35E -11	17.36

Tested values BEFORE fatigue: 01/02/80 page 1

	WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	75B		137.	.3397	5.067	.773	1.333	2.47E -11	17.30
	75B	1A-3	183.	.0235	4.384	.798	.973	2.08E -11	17.34
2.P3	75B		182.	.0190	4.255	.803	1.027	2.16E -11	17.34
	[illegible]		185	[illegible]	3.690	.821	.947	6.91E -11	16.99

Tested values BEFORE fatigue: 01/01/80 page 1

cell/vers	WAFER	struc/Area	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	75B		175.	.0283	2.863	.854	.813	1.58E -8	16.74
2.P6	75B	1A-2	176.	.1611	4.831	.790	1.253	2.14E -11	18.20
	75B		1.	*******	5.114	.782	1.507	7.09E -10	18.31
	75B		185.	.0192	4.729	.795	.960	2.70E -9	18.35

Tested values BEFORE fatigue: 01/01/80 page 1

	WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	75B		185.	.0152	4.314	.811	.960	3.37E -11	18.53
1.P6	75B	1-4	191.	.0710	4.165	.815	1.013	2.44E -11	18.40
	75B		192.	.0189	4.126	.817	1.013	2.34E -11	18.48
	75B		194.	.0180	3.443	.841	.933	3.54E -11	18.19

Tested values BEFORE fatigue: 01/01/80 page 1

	WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	75B		*****	-3.3170	4.957	.789	1.107	2.66E -11	18.49
2.P7	75B	1A-4	189.	.0196	4.753	.796	1.053	2.43E -11	18.56
	75B		-1.	*******	2.635	-.394	2.800	2.89E -11	-.75
	75B		192.	.0189	3.451	.836	.933	5.31E -11	17.63

Tested values BEFORE fatigue: 01/01/80 page 1

	WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	75B		186.	.0154	4.376	.811	.933	3.92E -11	18.78
1.P7	75B	1-5	191.	.0192	4.220	.816	1.053	2.01E -11	18.67
	75B		191.	.0187	4.408	.808	.960	2.14E -11	18.60
	75B		196.	.0188	3.435	.841	.893	2.07E -11	18.11

Tested values BEFORE fatigue: 01/01/80 page 1

	WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	75B		183.	.0161	5.247	.778	.933	2.47E -11	18.42
2.P8	75B	1A-5	181.	.0286	4.957	.786	1.400	1.55E -10	18.24
	75B		190.	.0181	4.667	.797	.973	5.34E -11	18.29
	75B		193.	.0188	3.576	.834	.907	9.46E -11	17.95

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Tested values BEFORE fatigue: 01/01/80 page 1

Cell/vers.	WAFER	STRUC/Area	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	69C		201.	.0168	4.455	.819	.920	3.60E -11	20.15
1.P2	69C		203.	.0195	4.259	.823	.973	3.12E -11	19.86
	69C	1-1	203.	.0197	4.078	.831	.960	9.82E -9	20.08
	69C		207.	.0203	3.325	.854	.960	8.73E -9	19.47

Tested values BEFORE fatigue: 01/01/80 page 1

	WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	69C		*****	-3.2920	4.933	.805	.933	3.96E -11	20.34
	69C		203.	.0196	4.235	.826	1.027	3.18E -11	20.11
2.P1	69C	1A-1	155.	*******	4.776	.809	1.000	1.08E -7	20.22
	69C		207.	.0184	4.306	.827	.933	2.82E -8	20.56

Tested values BEFORE fatigue: 01/01/80 page 1

	WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	69C		183.	.0155	4.024	.823	.867	3.66E -11	18.67
1.P3	69C		130.	*******	4.400	.822	.960	1.22E -6	20.34
	69C	1-2	201.	.0196	4.141	.827	.960	3.11E -11	19.84
	69C		191.	.0199	3.412	.843	.907	2.79E -11	18.31

Tested values BEFORE fatigue: 01/01/80 page 1

	WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	69C		184.	.0172	4.196	.817	.907	3.69E -11	18.78
2.P2	69C		186.	.0195	4.910	.794	.933	3.13E -11	18.93
	69C	1A-2	188.	.0199	4.392	.809	1.040	2.97E -11	18.56
	69C		190.	.0198	2.886	.861	.907	2.32E -11	17.91

Tested values BEFORE fatigue: 01/01/80 page 1

	WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	69C		59.	1.3534	3.976	.821	.920	2.32E -11	18.27
	69C		187.	.0430	4.024	.821	1.120	9.66E -11	18.43
1.P4	69C		189.	.0136	3.992	.822	.960	2.19E -11	18.45
	69C	1-3	192.	.0203	2.957	.857	.973	1.75E -11	17.76

Tested values BEFORE fatigue: 01/01/80 page 1

	WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	69C		182.	.0173	4.000	.821	.920	2.23E -11	18.29
2.P3	69C		163.	.0274	4.314	.810	1.333	2.04E -11	18.41
	69C	1A-3	188.	.0196	4.227	.812	2.107	2.05E -11	18.31
	69C		193.	.0267	3.027	.854	.907	1.69E -11	17.76

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER			Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	69C		199.	.0188	5.043	.799	.960	3.53E -11	20.09
1. P5	69C		202.	.0202	4.659	.811	1.000	2.82E -11	19.97
	69C	1A-4	183.	*******	4.949	.805	1.053	7.09E -7	20.38
oops	69C		212.	.0200	5.090	.798	.000	9.66E -7	20.09

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER			Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	69C		197.	.0163	4.988	.798	.973	3.06E -11	19.76
	69C		205.	.0206	3.937	.834	.960	2.60E -11	19.77
1. P6	69C	1-4	210.	.0211	4.000	.833	.987	1.07E -6	20.00
	69C		214.	.0211	49.274	-.001	1.013	6.23E -4	-.06

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER			Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	69C		186.	.0164	3.875	.828	.893	1.95E -11	18.67
	69C		192.	.0199	3.192	.853	.960	1.75E -11	18.47
1. P7	69C	1-5	193.	.0199	3.161	.855	.947	1.78E -11	18.60
	69C		195.	.0201	3.239	.852	.880	1.71E -11	18.65

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER			Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
	69C		187.	.0176	3.631	.837	.867	1.96E -11	18.69
	69C		190.	.0200	3.906	.827	.893	1.77E -11	18.61
2. P4	69C	1A-5	191.	.0202	3.929	.826	.880	1.80E -11	18.68
	69C		197.	.0208	3.067	.857	.880	1.67E -11	18.33

Tested values BEFORE fatigue: 01/01/80 page 1 Tested 3/31

WAFER	C (E-12)	tan(del)	DeltaP uC/cm^2	Rat1	Vc	log(I)	Ps-Pr
82B	.	*******	.012	.952	.000	9.04E -12	.24
82B	163.	.0174	3.016	.830	.840	2.17E -11	14.74
82B	.	*******	-.149	*****	.000	8.94E -12	.13
82B	1.	*******	-.169	*****	.000	9.18E -12	.13

	161	.0182	2.859	.836	.877	1.94E-11	14.57
B.						1.85E-11	14.91
D	160	.030	2.889	.838	.850		
E ?	146 ?		3.04	.82	.69	2.55E-11	13.7
F	160	.019	3.029	.832	.901	1.84E-11	14.99

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Tested values BEFORE fatigue: 01/01/80   page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82B	.	*******	.114	.121	.000	9.41E -12	.02
82B	147.	.0183	2.420	.850	.933	1.87E -11	13.67
82B	.	*******	-.008	3.000	.000	8.79E -12	.01
82B	1.	*******	.000	1.000	.000	8.88E -12	.33

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82B	.	*******	.000	1.000	.000	8.86E -12	.04
82B	169.	.0185	2.839	.841	.867	1.99E -11	15.06
82B	.	*******	.227	*****	.000	8.44E -12	-.14
82B	1.	*******	-.129	2.179	.000	8.31E -12	.24

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82B	.	*******	.024	.846	.000	8.98E -12	.13
82B	161.	.0185	3.039	.826	.867	1.90E -11	14.43
82B	.	*******	.000	1.000	.000	8.54E -12	.02
82B	1.	*******	-.208	-.710	.000	8.56E -12	.09

ted values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82B	.	*******	-.196	-.724	.000	8.88E -12	.08
82B	165.	.0183	2.980	.834	.880	1.77E -11	14.94
82B	.	*******	.145	.119	.000	8.26E -12	.02
82B	1.	*******	-.012	1.042	.000	8.23E -12	.29

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82D	.	*******	.024	.905	.000	8.82E -12	.22
82D	111.	.1068	-.192	-.361	.907	2.31E -11	.05
82D	.	*******	.043	.784	.000	7.91E -12	.16
82D	1.	*******	-.051	2.182	.000	8.08E -12	.09

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82D	.	*******	-.114	2.706	.000	8.75E -12	.18
82D	147.	.0678	2.706	.844	.827	1.94E -11	14.67
82D	.	*******	.102	.278	.000	8.77E -12	.04
82D	1.	*******	-.251	*****	.000	8.42E -12	.14

Tested values BEFORE fatigue: 01/01/80 page 1

Cap DeltaP

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82D	.	*******	-.165	*****	.000	8.37E -12	.09
82D	161.	.0184	2.980	.832	.933	1.82E -11	14.75
82D	.	*******	.271	*****	.000	7.52E -12	-.20
82D	1.	*******	.012	.500	.000	7.13E -12	.01

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82D	.	*******	-.016	-.333	.000	8.13E -12	.00
82D	.	*******	[illegible]	.851	.000	7.67E -12	.22
82D	.	*******	.208	*****	.000	7.43E -12	-.20
82D	1.	*******	.004	.952	.000	7.49E -12	.08

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82D	.	*******	.224	*****	.000	8.75E -12	-.15
82D	160.	.0182	3.188	.821	.907	1.77E -11	14.62
82D	.	*******	.188	*****	.000	7.29E -12	-.09
82D	1.	*******	.255	-.857	.000	6.81E -12	-.12

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82D		.	*******	.165	-.167	.000	1.12E -11	-.02
82D		173.	.0175	2.682	.853	.733	1.88E -11	15.61
82D		.	*******	.024	2.500	.000	7.47E -12	-.04
82D		1.	*******	-.086	-.222	.000	7.30E -12	.02

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82E		.	*******	-.125	-.778	.000	8.55E -12	.05
82E		18.	-.3066	3.749	.651	1.333	2.70E -11	7.00
82E		.	*******	.110	.000	.000	7.74E -12	.00
82E		1.	*******	.212	-.421	.000	8.29E -12	-.06

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82E		.	*******	.102	-.083	.000	8.55E -12	-.01
82E		1.	*******	.275	*****	1.240	3.68E -11	-.20
82E		.	*******	.204	-.625	.000	8.07E -12	-.08
82E		1.	*******	.086	.542	.000	7.89E -12	.10

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82E	?	.	*******	.102	.316	.000	7.56E -12	.05
82E		115.	.0176	2.565	.809	.680	2.14E -11	10.83
82E		.	*******	-.039	1.833	.000	8.04E -12	.09
82E		1.	*******	.165	.364	.000	8.15E -12	.09

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER		Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82E			*******	.110	-.556	.000	[illegible]	-.04

82E	1.	*******	.180	-.211	.000	8.21E -12	-.03

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82E	.	*******	.157	-.111	.000	8.37E -12	-.02
82E	147.	.0182	3.365	.803	.720	2.58E -11	13.68
82E	.	*******	.055	.774	.000	8.17E -12	.19
82E	1.	*******	.267	-.062	.000	7.82E -12	-.02

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82E	.	*******	.157	*****	.000	8.26E -12	-.08
82E	146.	.0183	2.714	.835	.653	2.52E -11	13.71
82E	.	*******	-.094	1.500	.000	7.06E -12	.28
82E	1.	*******	.078	.286	.000	8.30E -12	.03

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82F	.	*******	.118	-.667	.000	8.51E -12	-.05
82F	145.	.0191	2.753	.831	.800	2.06E -11	13.52
82F	.	*******	-.047	.500	.000	8.04E -12	-.05
82F	1.	*******	-.196	*****	.000	8.16E -12	.18

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82F	.	*******	.118	-.500	.000	1.09E -11	-.04
82F	156.	.0189	3.239	.818	.960	1.44E -11	14.56
82F	.	*******	.157	.167	.000	8.10E -12	.03
82F	1.	*******	-.173	1.917	.000	8.21E -12	.36

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82F	.	*******	.102	-.083	.000	8.55E -12	-.01
82F	1.	*******	.275	*****	1.240	3.68E -11	-.20
82F	.	*******	.204	-.625	.000	8.07E -12	-.08
82F	1.	*******	.086	.542	.000	7.89E -12	.10

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	-12)	tan(del)	uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82F	[illegible]	*******	.000	1.000	.000	9.83E -12	-.01
82F	166.	.0189	3.514	.820	.880	2.05E -11	16.05
82F	.	*******	.220	*****	.000	8.95E -12	-.13
82F	1.	*******	-.235	*****	.000	7.98E -12	.25

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82F	.	*******	.196	*****	.000	8.51E -12	-.10
82F	167.	.0189	2.580	.856	.920	1.93E -11	15.37
82F	.	*******	.133	*****	.000	9.50E -12	-.10
82F	1.	*******	-.016	1.400	.000	9.34E -12	.05

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
82F	.	*******	.141	-.286	.000	8.68E -12	-.03
82F	165.	.0194	3.059	.835	.947	1.95E -11	15.46
82F	.	*******	.055	.759	.000	9.14E -12	.17
82F	1.	*******	.039	.500	.000	9.15E -12	.04

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TEST FILM TRAVELER   Krysalis Confidential   April 10, 1987

FILM ID	SUBSTRATE	BEL	TEL	BAKE	ANNEAL	DAY MADE
7096C	Th Oxide	B66-4	LODM	2@400	30@650inO2	04/06/87

NOTES:Excess Pb study
G7090A(8/40/60,+0);8cts;6 days old

FILM ID	SUBSTRATE	BEL	TEL	BAKE	ANNEAL	DAY MADE
7096D	Th Oxide	B66-4	LODM	2@400	30@650inO2	04/06/87

NOTES:Excess Pb study
G7091(8/40/60,+30);8cts;5 days old

FILM ID	SUBSTRATE	BEL	TEL	BAKE	ANNEAL	DAY MADE
7096E	Th Oxide	B66-4	LODM	2@400	30@650inO2	04/06/87

NOTES:New composition
G7092(6/50/50,+10);8cts;4 days old

FILM ID	SUBSTRATE	BEL	TEL	BAKE	ANNEAL	DAY MADE
7096F	Th Oxide	B66-4	LODM	2@400	MufFur650	04/06/87

NOTES:Fast ramp study
G7047(8/40/60,+10);8cts;49 days old

FILM ID	SUBSTRATE	BEL	TEL	BAKE	ANNEAL	DAY MADE
7096G	Th Oxide	B66-4	LODM	2@400	2"/'-650°	04/06/87

NOTES:Slow ramp study
G7047(8/40/60,+10);8cts;49 days old

FILM ID	SUBSTRATE	BEL	TEL	BAKE	ANNEAL	DAY MADE
7096H	Th Oxide	B66-4	LODM	2@400	30@650inO2	04/06/87

NOTES:Control for 7096I
G7072(3/40/60,+10);8cts;24 days old

FILM ID	SUBSTRATE	BEL	TEL	BAKE	ANNEAL	DAY MADE
7097A	Th Oxide	B66-4	LODM	2@400	30@650inO2	04/07/87

NOTES:2X std. sol-gel concentration; spin 4 coats at 4000 rpm
G7090B(8/40/60,+30*);4cts;7 days old

Note 4 coats of this sol-gel equivalent to 8 coats normal gels; ~ 4300 Å

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Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
96C	118.	.0138	3.286	.775	1.053	1.06E -10	11.30
96C	133.	.0149	2.443	.832	.813	4.58E -11	12.08
96C	.	*******	.020	.667	.000	4.73E -12	.04
96C	1.	*******	.012	.906	.000	6.54E -11	.11

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
Retest 96C	109.	.2448	1.243	.882	.720	1.11E -10	9.33
96C	125.	.0138	1.353	.887	.707	1.03E -10	10.67
96C	1.	*******	.004	.964	.000	1.94E -11	.11
96C	113.	.0149	1.345	.879	.800	9.32E -11	9.75

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
96D	157.	.0190	3.561	.815	.853	9.99E -10	15.67
96D	162.	.0227	3.133	.827	.880	1.06E -8	15.00
96D	1.	*******	.024	.769	.000	1.04E -11	.08
96D	164.	.0234	3.090	.830	.867	8.61E -10	15.05

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
96E	194.	.0122	5.600	.774	1.000	1.49E -11	19.13
96E	182.	.0172	4.357	.786	1.013	1.15E -11	15.99
96E	1.	*******	.012	.930	.000	6.07E -12	.16
96E	208.	.0185	4.569	.792	1.000	1.20E -11	17.39

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
96F	154.	.0128	4.722	.772	.947	1.55E -11	15.97
96F	162.	.0177	3.392	.813	.920	1.25E -11	14.77
96F	164.	.0178	3.455	.810	.933	1.24E -11	14.68
96F	2.	*******	-.012	1.079	.000	6.76E -12	.16

Tested values BEFORE fatigue: 01/01/80 page 1

Retest

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
96F	14[illegible]	.0151	4.459	.773	1.000	1.59E -11	15.21
96F	16[illegible]	.0161	4.200	.791	.920	1.34E -11	15.93
96F	165.	.0161	4.263	.788	1.000	1.39E -11	15.82
96F	2.	*******	.039	.841	.000	6.81E -12	.21

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
96G	147.	.0191	4.404	.773	1.093	1.89E -11	15.01
96G	149.	.0190	4.204	.779	1.080	1.59E -11	14.78
96G	153.	.0191	4.322	.776	1.080	1.80E -11	14.97
96G	2.	*******	-.004	1.020	.000	7.27E -12	.20

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
96H	122.	.0160	9.647	.612	2.093	2.05E -11	15.20
96H	133.	.0195	8.894	.642	1.987	1.73E -11	15.97
96H	132.	.0197	9.133	.634	2.000	2.42E -11	15.80
96H	135.	.0204	9.518	.619	2.080	1.97E -11	15.45

Tested values BEFORE fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
97A	156.	.0210	4.561	.774	1.080	7.87E -10	15.63
97A	161.	.0206	4.690	.770	1.080	2.02E -10	15.67
97A	162.	.0201	4.518	.775	1.080	1.46E -10	15.58
97A	164.	.0209	4.047	.790	1.000	1.42E -10	15.22

Tested values ~~BEFORE~~ after fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
97A	156.	.0210	4.561	.774	1.080	7.87E -10	15.63
97A	161.	.0206	4.690	.770	1.080	2.02E -10	15.67
97A	162.	.0201	4.518	.775	1.080	1.46E -10	15.58
97A	164.	.0209	4.047	.790	1.000	1.42E -10	15.22

Tested values ~~BEFORE~~ fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
96H	124.	.0217	4.145	.762	1.480	2.42E -11	13.25
96H	125.	.0194	4.188	.758	1.480	5.72E -11	13.15
96H	125.	.0190	4.137	.761	1.467	1.93E -11	13.17
96H	127.	.0194	4.243	.758	1.480	2.05E -11	13.29

Tested values ~~BEFORE~~ fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
96G	141.	.0187	1.671	.883	.840	2.00E -11	12.57
96G	137.	.0171	1.686	.877	.840	1.74E -11	11.98
96G	137.	.0171	1.663	.878	.840	1.66E -11	12.02
96G	143.	.0172	1.780	.876	.840	1.70E -11	12.53

Tested values ~~BEFORE~~ fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
96F	148.	.0161	1.573	.893	.760	1.64E -11	13.09
96F	73.	.0146	.792	.891	.693	1.26E -11	6.48
96F	146.	.0146	1.557	.891	.760	1.38E -11	12.78
96F	149.	.0150	1.639	.888	.760	1.38E -11	12.99

Tested values ~~BEFORE~~ fatigue: 01/01/80 page 1

Tested values ~~BEFORE~~ after fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
96E	171.	.0164	2.553	.853	1.080	3.44E -11	14.82
96E	63.	.0172	1.063	.837	1.080	1.06E -11	5.47
96E	186.	.0155	2.490	.865	1.160	1.46E -11	15.90
96E	162.	.0157	2.227	.861	1.160	1.28E -10	13.76

Tested values ~~BEFORE~~ fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
96D	153.	.0249	1.694	.885	.840	9.74E -10	13.09
96D	154.	.0242	1.804	.880	.760	3.19E -8	13.21
96D	152.	.0242	1.686	.885	.760	4.25E -9	13.03
96D	155.	.0238	1.722	.885	.760	1.22E -9	13.26

Tested values ~~BEFORE~~ fatigue: 01/01/80 page 1

WAFER	Cap (E-12)	tan(del)	DeltaP uC/cm^2	Ratl	Vc	log(I)	Ps-Pr
96C	116.	.0142	1.051	.905	.653	7.17E -10	9.98
96C	80.	.0136	.671	.910	.560	1.54E -10	6.81
96C	24.	.0115	.188	.918	.267	8.15E -11	2.11
96C	118.	.0136	1.027	.907	.640	2.42E -10	10.06

5

Minutes of Device Process Request Scheduling Meeting
4/15/87

Purpose of meeting: Establish priorities for individuals between now and Jun 1, 87 as well as schedule the test devices to be requested from Process.

Results:

Approved equipment acquisitions:

Richard - AT for the P-Cad sftware
1.5 MIPS to 2.5 MIPS diskless Sun workstation for CAD system
4 terminals, 4 1200 BAUD terminal modems, and 2 2400 BAUD base modems

Mike - Gets the Compaq for the LTF system
Can acquire an HP8116 pulse generator for the LTF
Can use one of the rented Tek 2430 digital oscilloscopes

Wayne - nothing!

We determined that any test structures we want to examine should be in the F1 strucutres if possible. Also, all tests we want involve the LTF system so that the limited test throughput of the system is an issue. The major characteristics we need to test are

Composition,
Thickness of the capacitor,
and buffer layers in the capacitor.

Because of the large numbers of test combinations that can be generated from this list, we will attempt to hold off the thickness and buffer experiments until a narrowed scope of composition is achieved. However, if Process can produce more structures than we request as a result of the above limitation, we can add the thickness and buffer experiments earlier.

According to Mike, the bonder will not be up until May 5. The FAST LTF system will be up on May 22 if Mike is the only one working on it. Wayne's priorities were adjusted to allow him to assist Mike on bringing the FAST LTF and bonder up.

We looked at process scheduling and decided to ask for three compositions on F1 structures to be delivered in two weeks. We will put them into the LTF as they become packaged. The compositions are:

6/50/50
15/0/100
8/20/80.

Whether we do any more than that depends on the Process groups throughput.

LTF testing throughput:

Until May 22, we will do one test day a week and can test up to 42 packages a day. 32 are committed now.

After May 22, or when the FAST LTF is up, we can test roughly 100 packages/day. We will also have a hot capability by that time. Cold temp and temp cycling will have to wait for the new building.

ACTION ITEMS:

Wayne - Establish standard tests
Help Mike bring up FAST sftware
Work on PEM, Due Date: Jun 1
Look at grain boundry enhancement for cross section work

Richard - Complete F2 masks if necessary
Order number cruncher
Get HSPICE or SIMON
Plan out software development and verification plan with Chris
Order terminals
Order AT for P-Cad

Mike - Bring bonder up
Bring FAST software up
Bring up temp chambers
Bring up separate LTF system
Get next LTF packages bonded (in-house)
Check on scribe suitability
Order in-house scribe if it is useful
Manage F2 masks and fabrication

Joe - Complete polarization measurement system for 512
Look into drivers

Postscript:

I talked to Bill Shepherd. They can do 8 F1's a week on average. They will require 3 to 4 of them for their stuff. We can have 4 to 5 each week. We have to consider which of their experiments will also go on the LTF when we consider the LTF testing saturation for the next 5 weeks. (Meeting required)

Bill Miller stated that there may be room to set up the cold and hot chambers at the university if they get more room from Jungling. Mike should foolow this up with Bill.

It may be July before we can set up anything at the new building so plan accordingly.

JTE

6

KRYSALIS CONFIDENTIAL

TO: Distribution

DATE: April 24, 1987

FROM: Michael Cordoba

SUBJECT: MEASUREMENT OF RESISTANCE TEL OVER FES (Before Anneal)

++

TELFES.TXT

Bill S. provided us with two 512 wafers to measure the resistance of the serpentine structure of TEL over FES. The wafers were 7098E and 7098F. We measured 20 sites on each wafer, see the attached results.

The resistance was generally linear but varied a great deal across the wafer, particularly for wafer 7098E, variations were from 300 ohms to 690 ohms. Resistance on wafer 7098F was lower and the range was smaller (291 to 396 ohms).

By the way, the value of resistance expected for the serpentine is in the order of 257 ohms, since there are 257 squares and the sheet resistance of the TEL is 1 ohm/square.

Notice also the FES capacitor (100x100 μm^2) hysteresis curves (measured by Anita) show variations across the wafer — it appears that the center of the wafer has a lower ΔP than the edges (Left + Right sides of wafer) — refer to pictures).

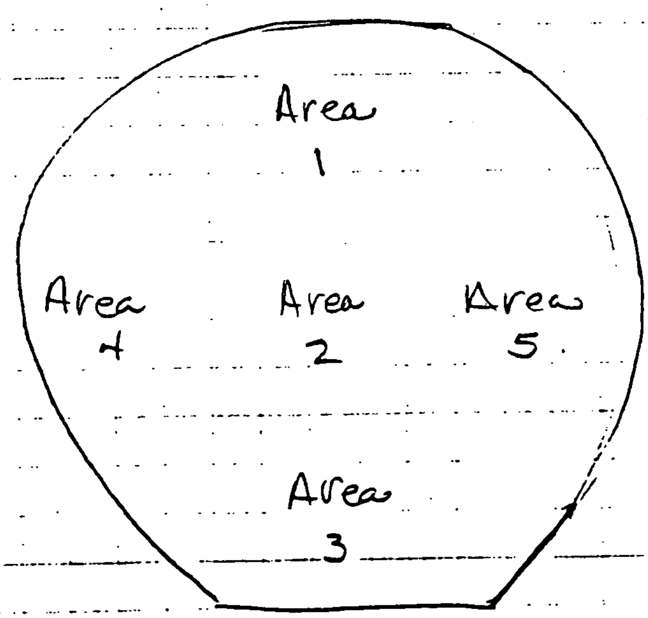
4/22/07

	R	V	R	V
7098E Area 1	647Ω	5		
	690Ω	5		
	462Ω	5		
	687Ω	5		
	618Ω	5		
Area 2	341Ω	5		
	329Ω	5		
	329Ω	5		
	318Ω	5		
	310Ω	5		
Area 3	348Ω	5		
	380Ω	5		
	510Ω	1	1×10^6	6
	355Ω	5		
	456Ω	5		
Area 4	359Ω	5		
	332Ω	5		
	330Ω	5		
	424Ω	5		
	397Ω	5		
Area 5	432Ω	5		
	455Ω	5		
	444Ω	5		
	428Ω	5		
	402Ω	5		

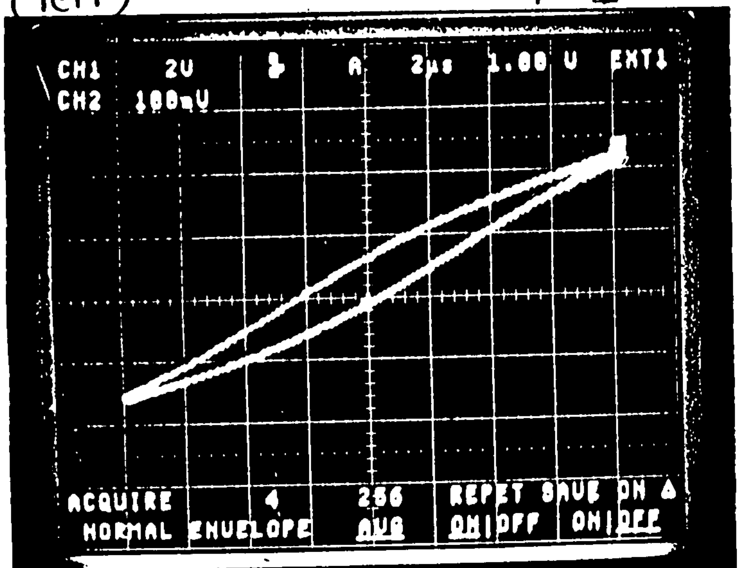
7098F Area 1	526Ω	5
	421Ω	5
	375Ω	5
	417Ω	5
	581Ω	5

7098E

	R	V		R	V
Area 2	295Ω	5			
	293Ω	5			
	293Ω	5			
	291Ω	5			
	304Ω	5			
Area 3	313Ω	5			
	323Ω	5			
	340Ω	5			
	350Ω	5			
	339Ω	5			
Area 4	361Ω	5			
	340Ω	5			
	336Ω	5			
	338Ω	5			
	370Ω	5			
Area 5	324Ω	5			
	350Ω	5			
	396Ω	5			
	362Ω	5			
	329Ω	5			

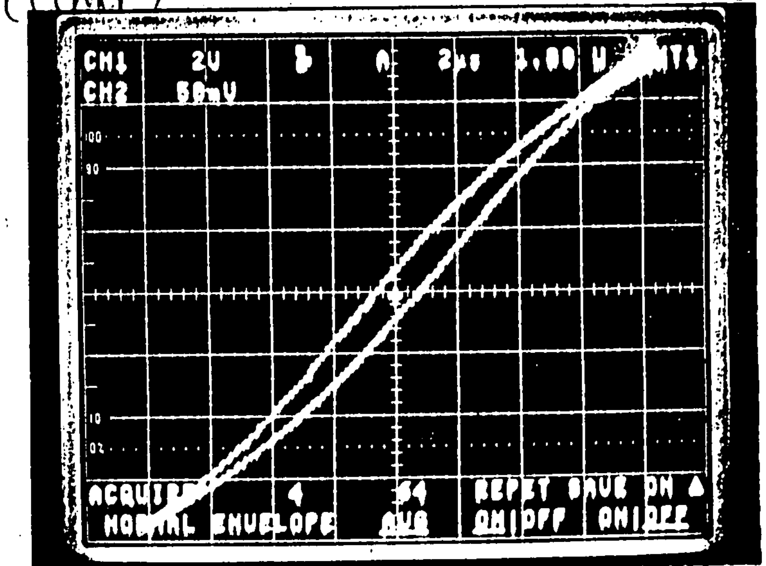


(left) Pos 1



4/27/87 8V 7098F

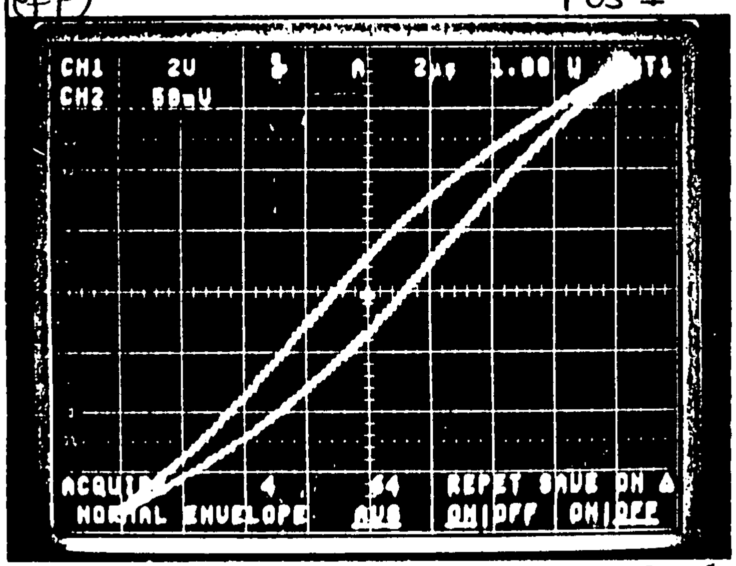
(center) Position 2



4/27/87 8V 7098F

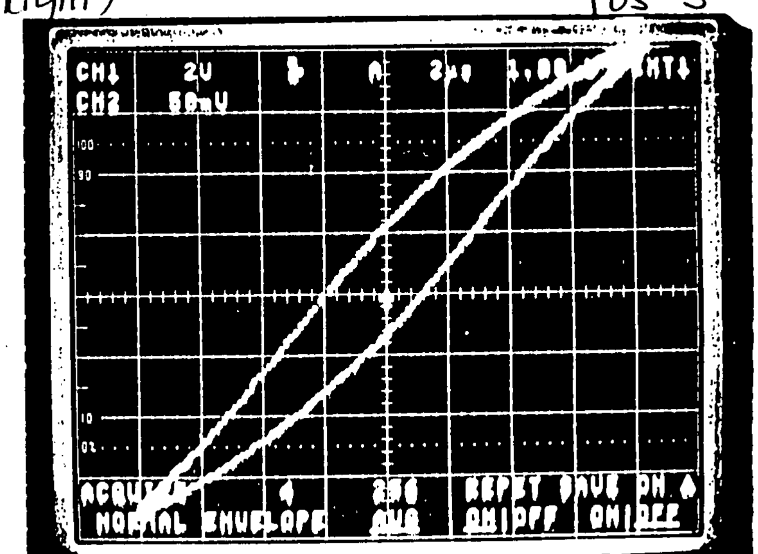
100 X 100 CAPACITOR

(left) Pos 1



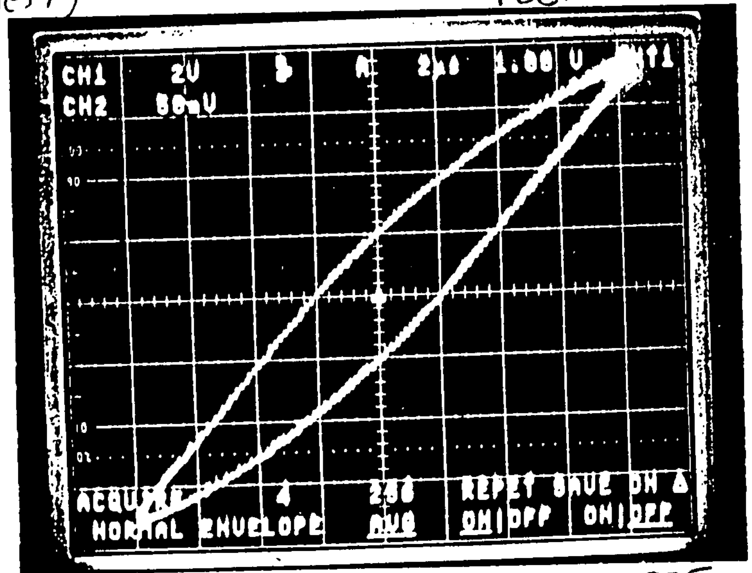
4/27/87 8V 7098F

(Right) Pos 3



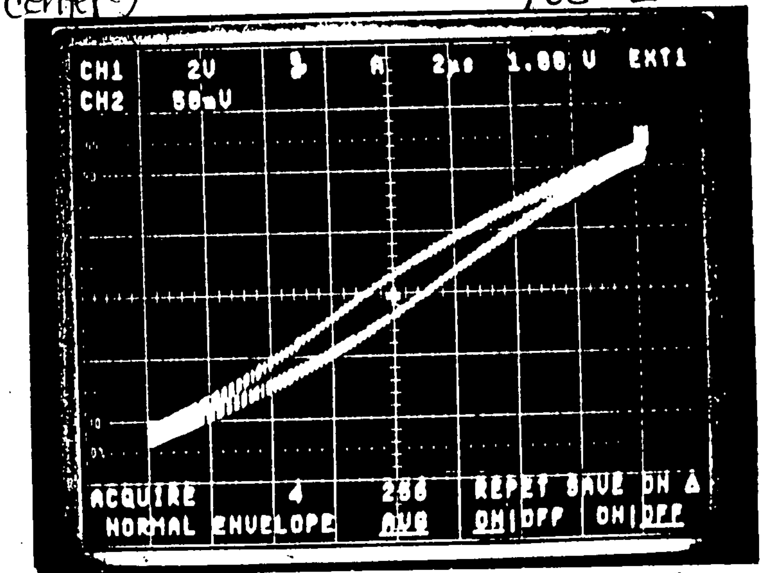
4/27/87 8V 7098F

(left) Pos. 1



4/27/87 8 V 7098E

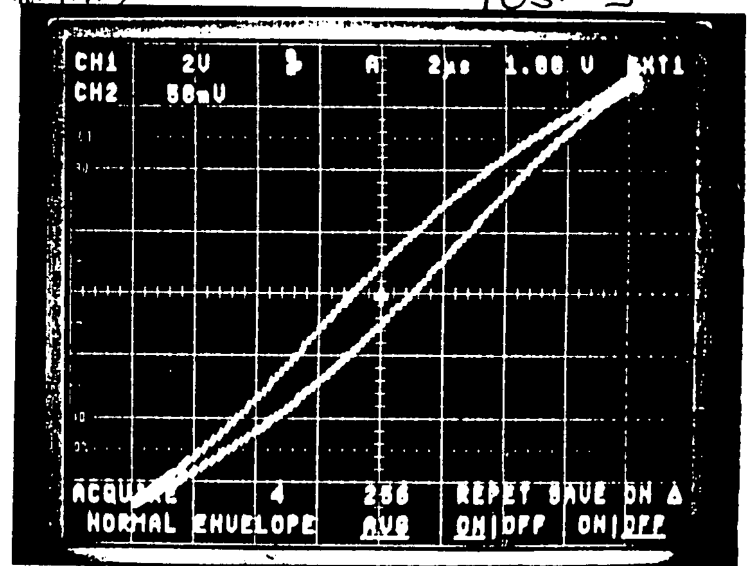
(center) Pos 2



4/27/87 8V 7098E

100 x 100 CAPACITOR

(Right) Pos. 3



4/27/87 8V 7098E

KRYSALIS CORPORATION

TO: Joe Evans DATE: April 28, 1987

FROM: Michael Cordoba

SUBJECT: LTF as a Function of Stress Pulse and Composition

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fat1.txt

Introduction-

As we are well aware Long Term Fatigue (LTF) is one of the critical issues facing us - and the literature on this subject besides being scarce offers very conflicting information. The purpose of this study is to determine if we can make a long term reliable memory. This is the beginning of a series of memos which will look at the issue of LTF in varios compositions of PLZT. This first memo is a preliminary look at Delta-P as a function of stress pulse and composition.

The first thrust of the LTF system is to look at fatigue at room temperature. I've placed 36 die on the LTF system at room temperature. The actual die and their composition is specified in Table 1 below.

table 1

Chip Label	Lot #	Structure	Composition
A	7076A	1	3/40/60
B	7076B	1	0/50/50
C	7069D	1	8/40/60
D	7075A	1A	8/40/60
E	7076A	1A	3/40/60
F	7076B	1A	0/50/50
G	7069D	1A	8/40/60
H	7075A	1	8/40/60

The stress board is divided into 5 columns which can have 5 different signals per column. There are 8 chips (i.e. chips A thru H) per column on columns 1 thru 4 and 4 chips on column 5 (i.e. chips A, B, C, and H). The actual signals applied to each column is specified below.

column 1 - square wave 8V to -8V @ 10 KHz.
column 2 - square wave 8V to 0V @ 10 KHz.
column 3 - DC of 8 volts.
column 4 - no stress. Control

column 5 - 10 % duty cycle of column 1 with a sinusoidal wave.

Results -

- Fatigue is flat for columns 2, 3 and 4. That is when the memory is not switched.

- Fatigue is worse when memory is switched from a zero to one and back again. The plots at the end of this report are for columns 1 and 5.

- It appears that the fatigue rate is not duty cycle dependent. In other words, column 5 which is flipped 10 times less often doesn't fatigue with a 10 fold decrease in slope. In fact, in some cases it looks like it fatigues at very close to the same rate as column 1.

- Data with and without Aluminum on top of capacitor is practically identical for all compositions tested.

- It appears that the 8/40/60 fatigue is leveling off at 2 uC/cm^2. This is significant !

- The capacitor sigma is less than 1% of the DELTA-P before fatigue and usually becomes less than .5% of DELTA-P after fatigue.

- Delta-P appears to follow a normal distribution (refer to figure 1).

Speculations and Conclusions ?

It appears that the fatigue rate flattens out after a period of time for 8/40/60. This is good news ! Maybe the other materials will also flatten out.

There seems to be two mechanisms of fatigue (I'm referring to the 8/40/60 material). One which occurs very rapidly, so rapidly that we do not see a duty cycle dependence, sort of an " infant fatigue " of domains which with time no longer switch their polarization. And then what is left is the " intrinsic fatigue " rate of domains which " appear " to be able to continue switching.

Appendix -

figure 1 - Histogram of initial Delta-P vs # of samples of 3/40/60, step size is .1 uC/cm^2.

figure 2 - Plot of Delta-P vs Log[hours] of 3/40/60 for column 1 (*) vs column 5 (#) with structure 1.

figure 3 - Plot of Delta-P vs Log[hours] of 0/50/50 for column 1 (*) vs column 5 (#) with structure 1.

figure 4 - Plot of Delta-P vs Log[hours] of 8/40/60 for column 1 (*) vs column 5 (#) with structure 1.

figure 5 - Plot of Delta-P vs Log[hours] of 8/40/60 for column 1 (*) with structure 1A.

figure 6 - Plot of Delta-P vs Log[hours] of 3/40/60 for column 1 (*) with structure 1A.

figure 7 - Plot of Delta-P vs Log[hours] of 0/50/50 for column 1 (*) with structure 1A.

figure 8 - Plot of Delta-P vs Log[hours] of 8/40/60 for column vs column 5 (#) with structure 1A.

figure 9 - Plot of Delta-P vs Log[hours] of 8/40/60 for column 1 (*) vs column 5 (#) with structure 1.

Figure 1

3/40/60 Histogram

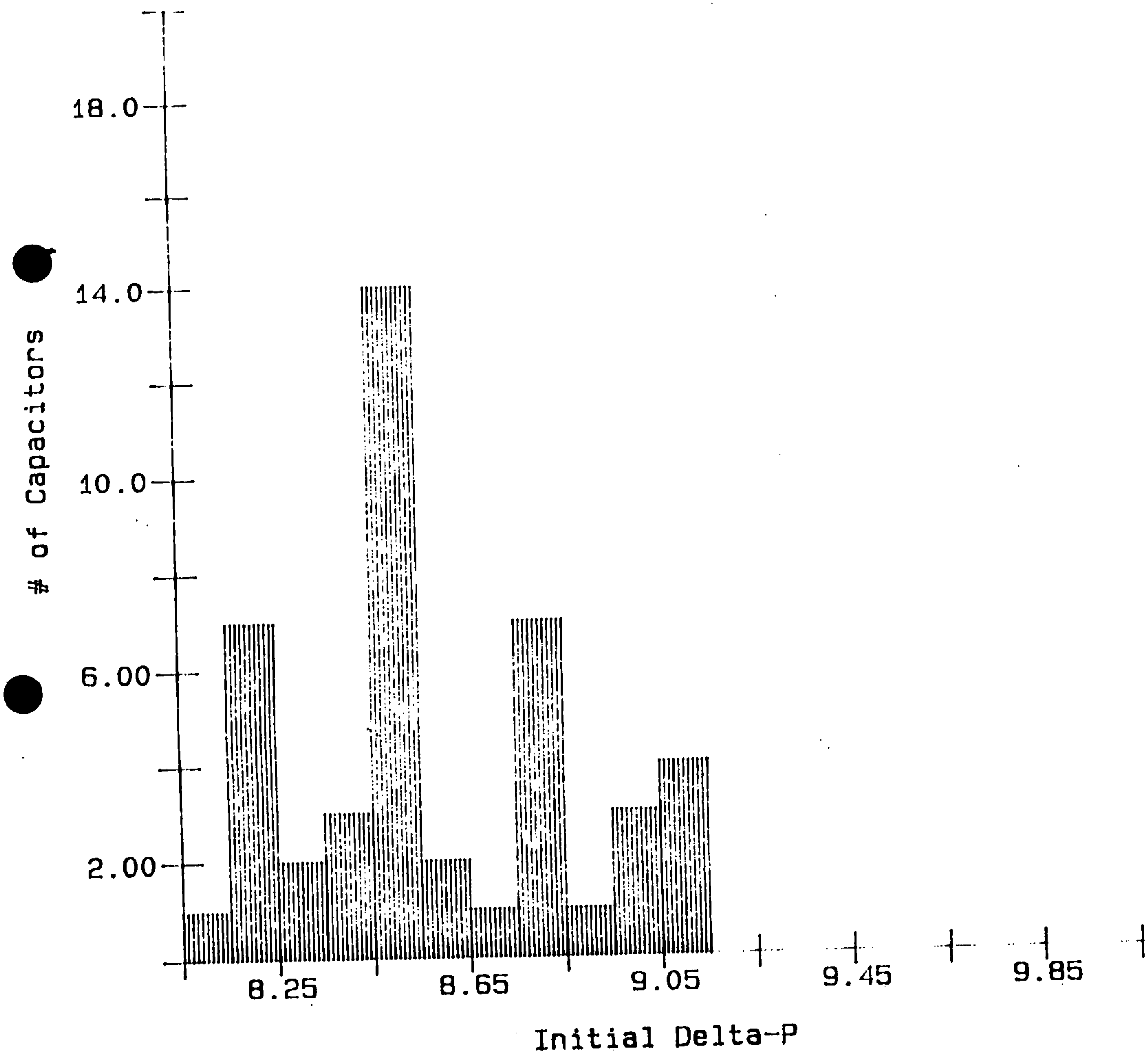
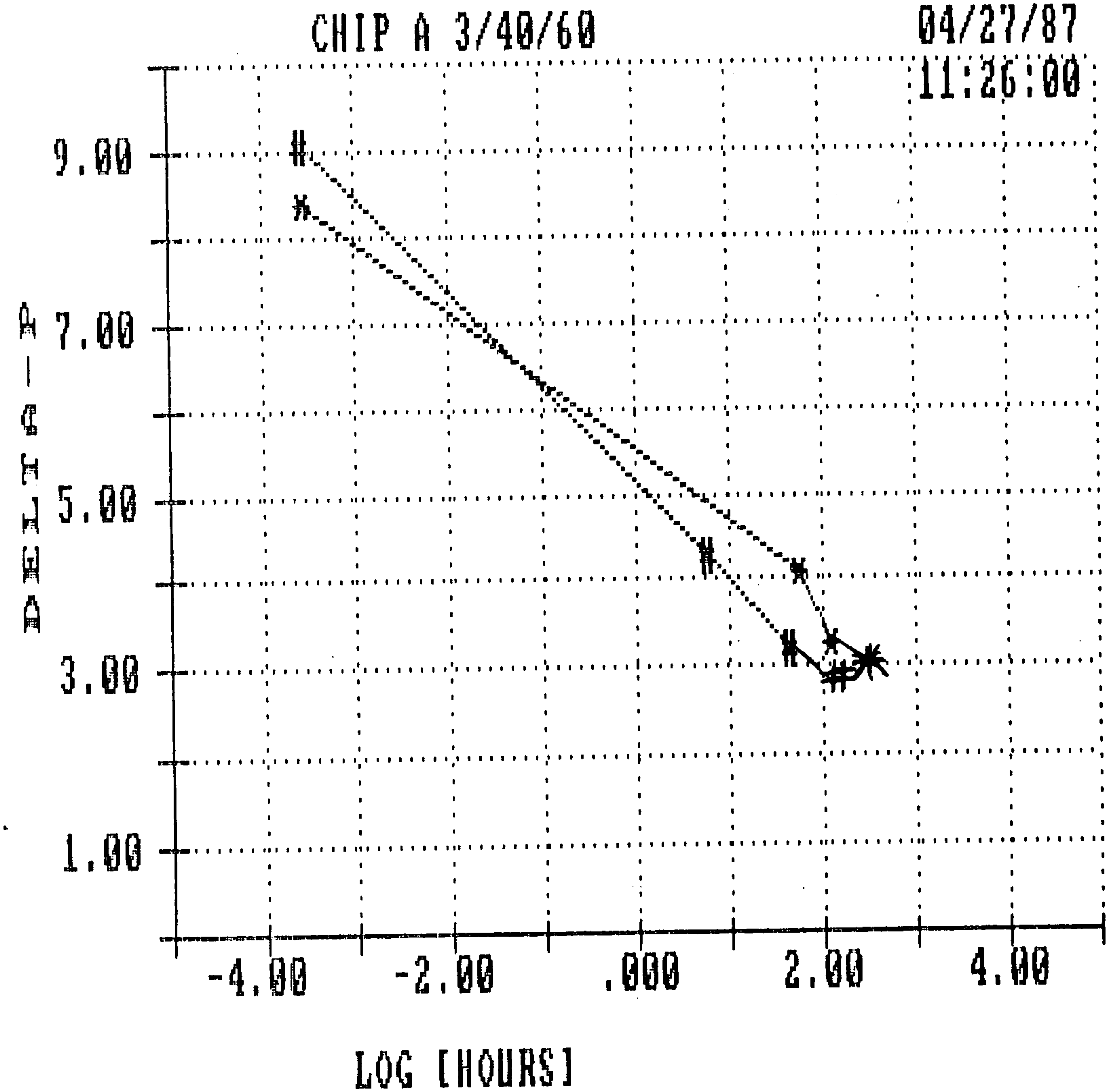
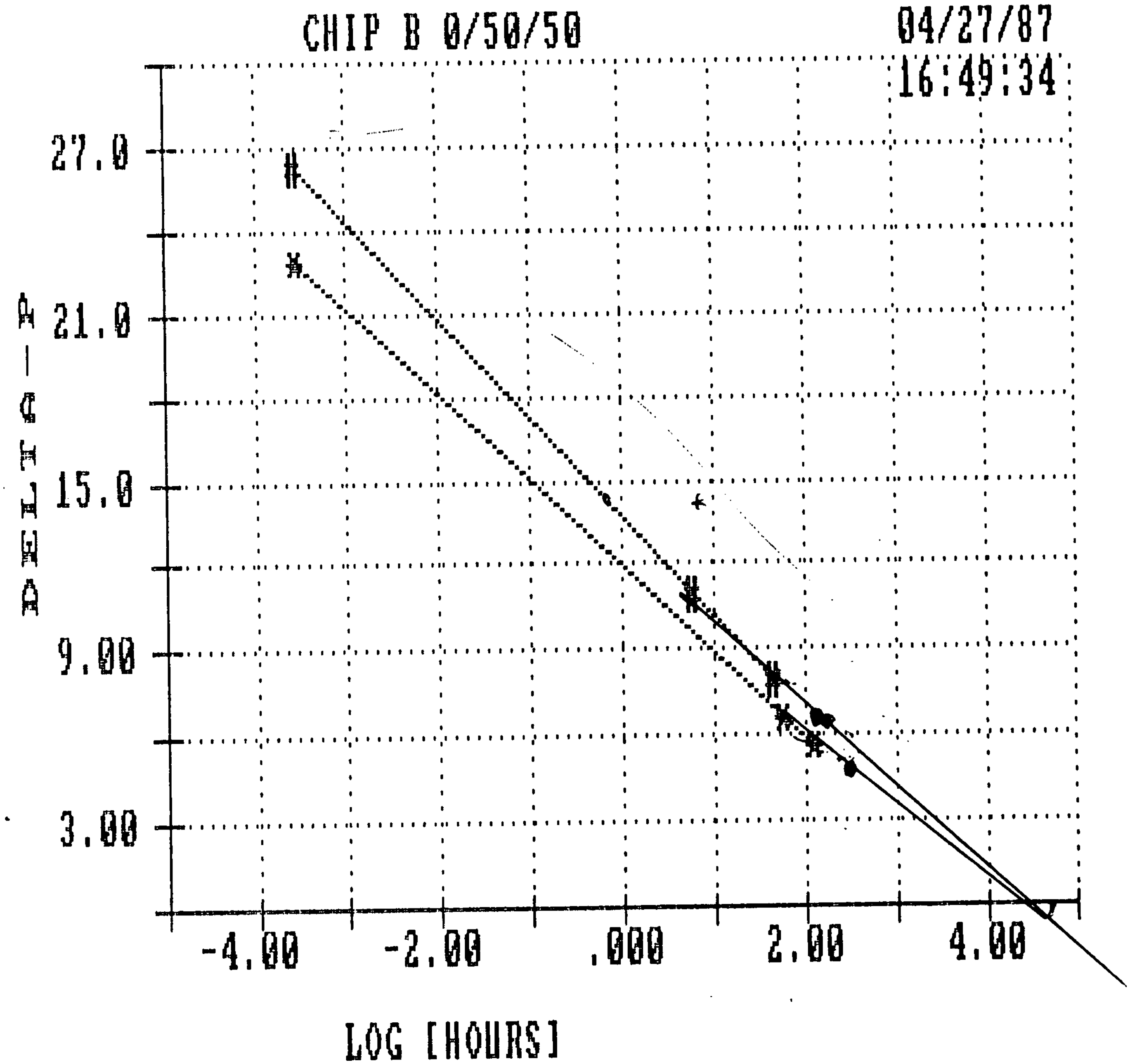


Figure 2



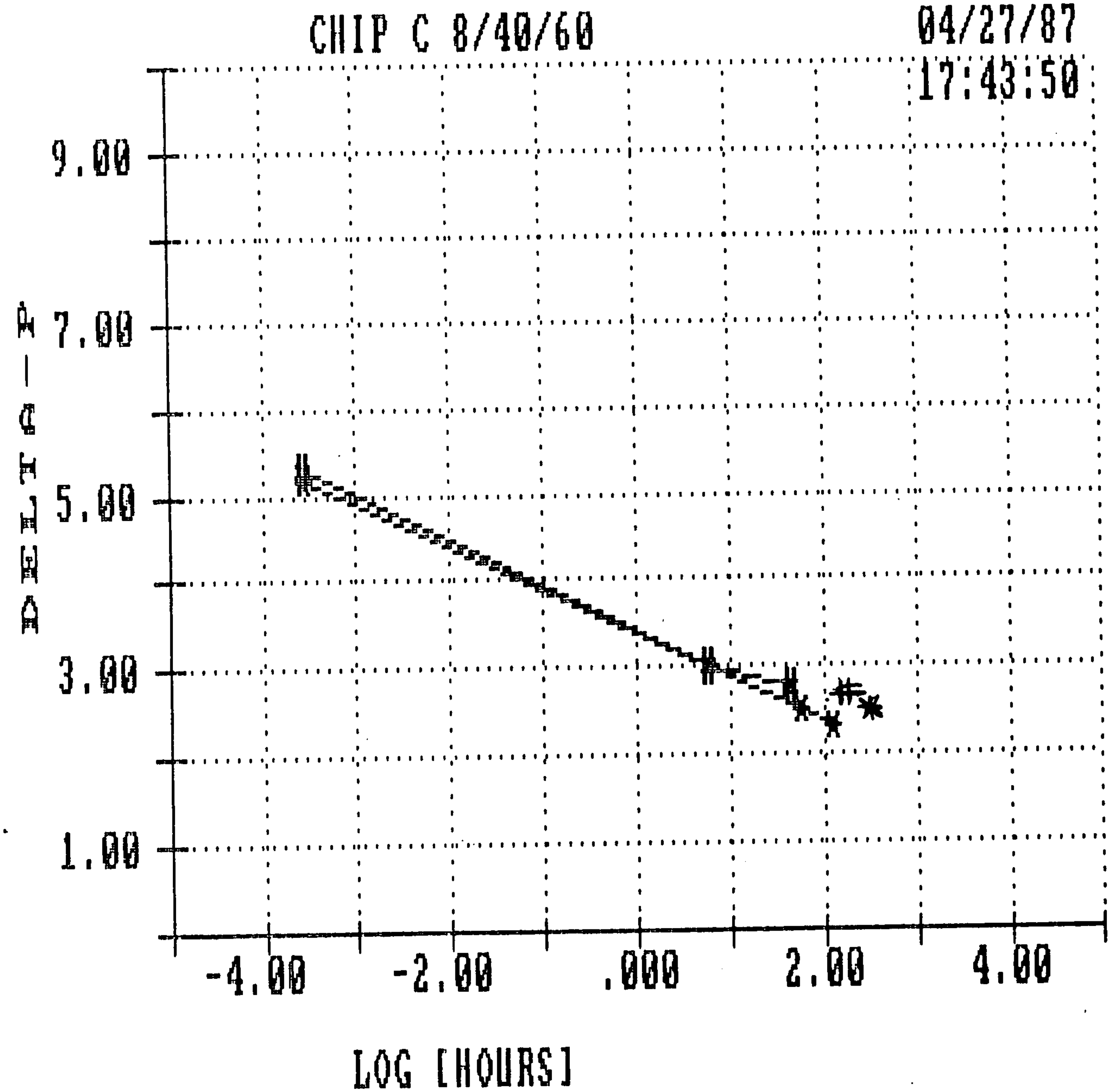
CHIP A 3/40/60
04/27/87
11:26:00
9.00
7.00
5.00
3.00
1.00
DELTA - A
-4.00
-2.00
.000
2.00
4.00
LOG [HOURS]

Figure 3



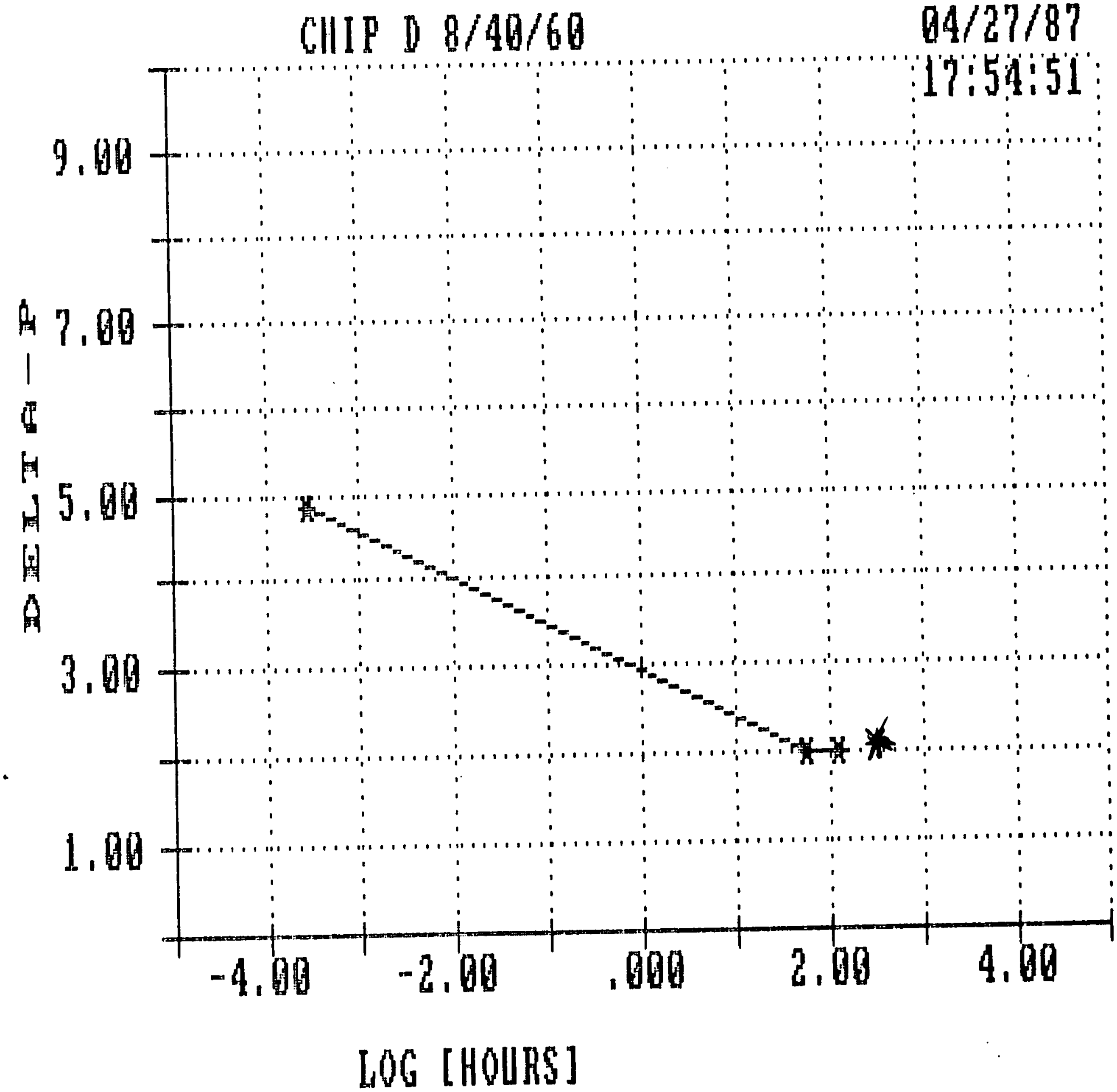
CHIP B 0/50/50
04/27/87
16:49:34
27.0
21.0
15.0
9.00
3.00
DELTA-P
-4.00
-2.00
.000
2.00
4.00
LOG [HOURS]

Figure 4



CHIP C 8/40/60
04/27/87
17:43:50
9.00
7.00
5.00
3.00
1.00
DELTA-R
-4.00
-2.00
.000
2.00
4.00
LOG [HOURS]

Figure 5



CHIP D 8/40/60
04/27/87
17:54:51
9.00
7.00
5.00
3.00
1.00
DELTA-P
-4.00
-2.00
.000
2.00
4.00
LOG [HOURS]

Figure 6

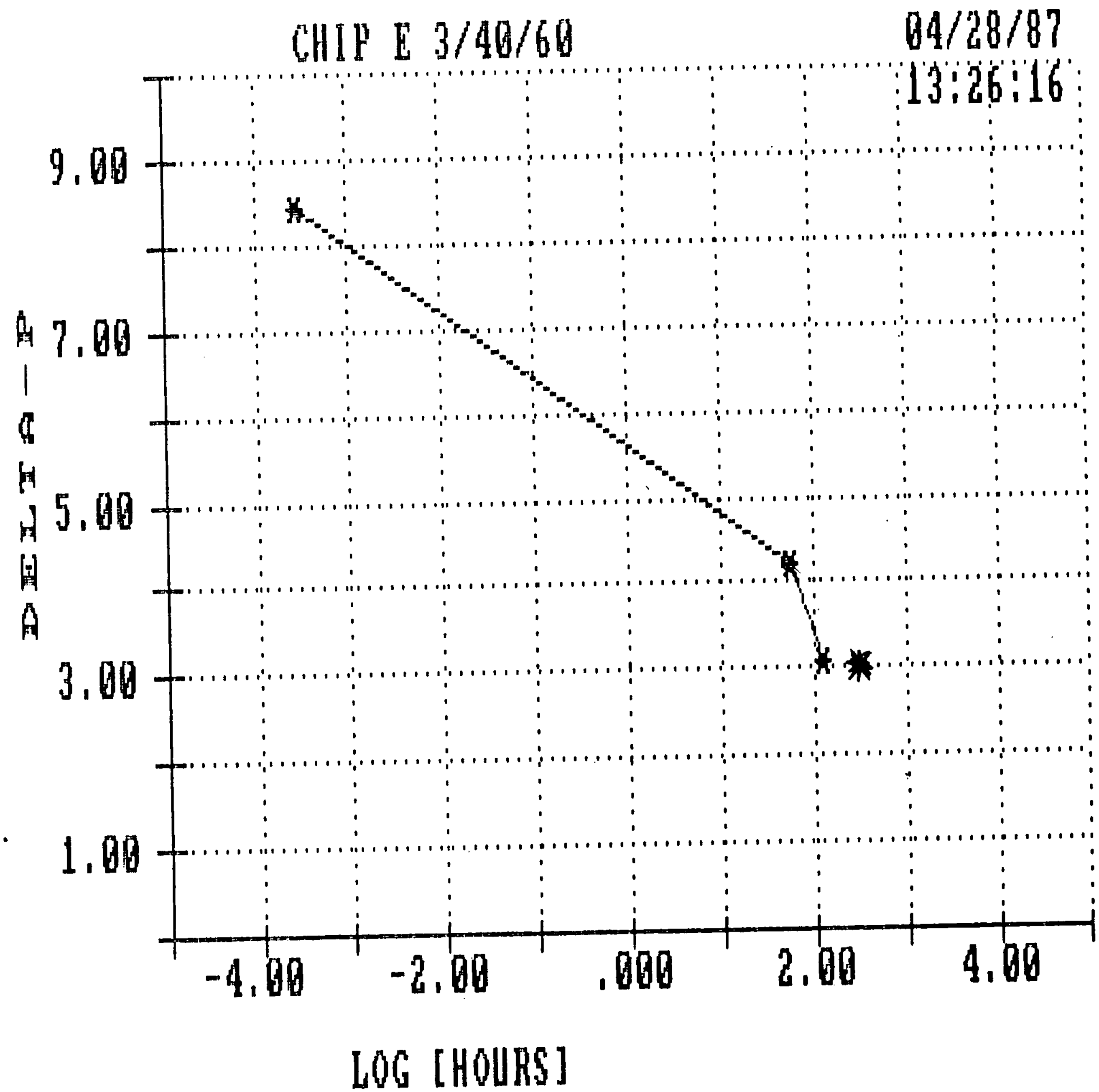

CHIP E 3/40/60
04/28/87
13:26:16
9.00
7.00
5.00
3.00
1.00
DELTA - A
-4.00
-2.00
.000
2.00
4.00
LOG [HOURS]

Figure 7

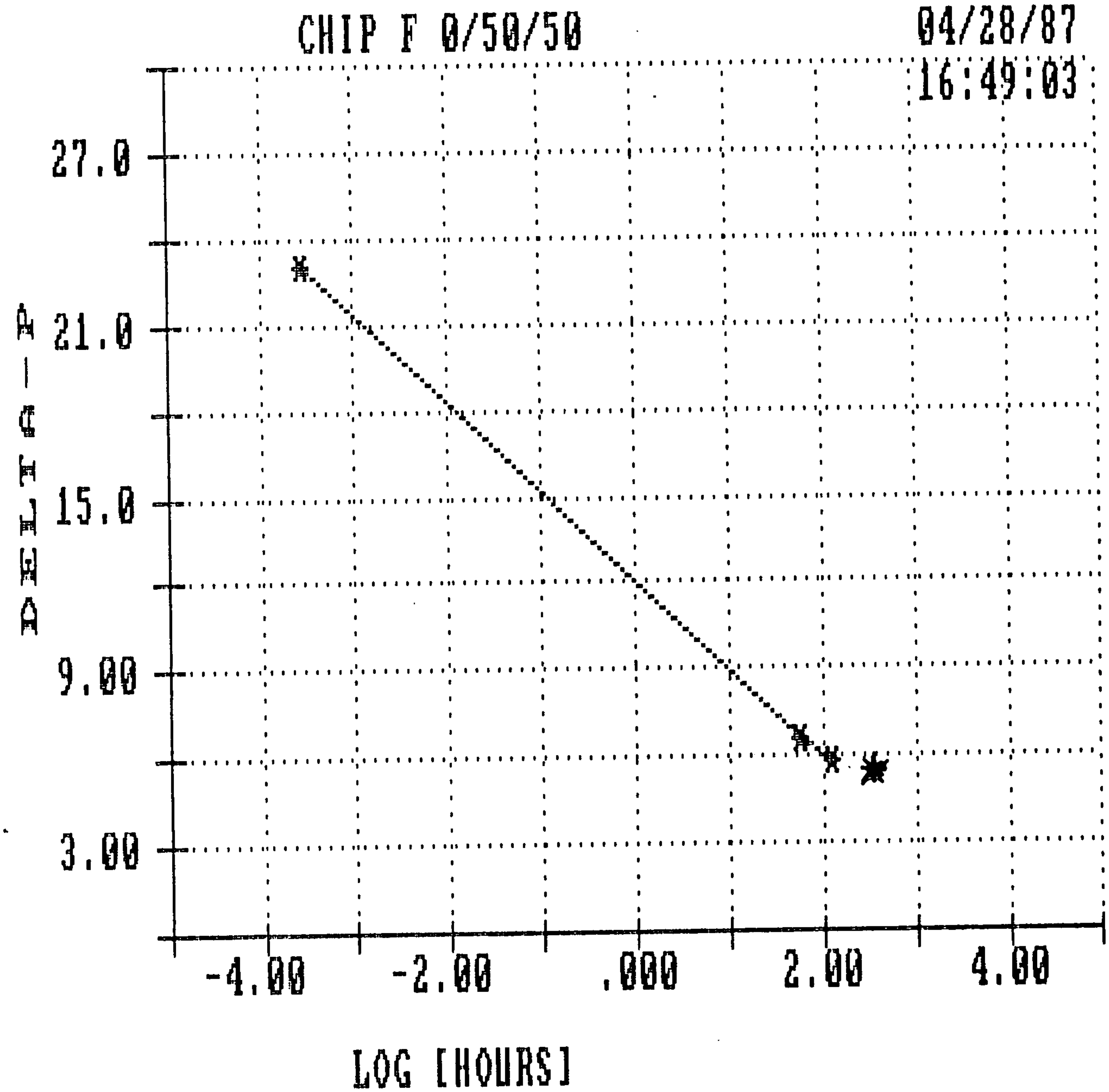
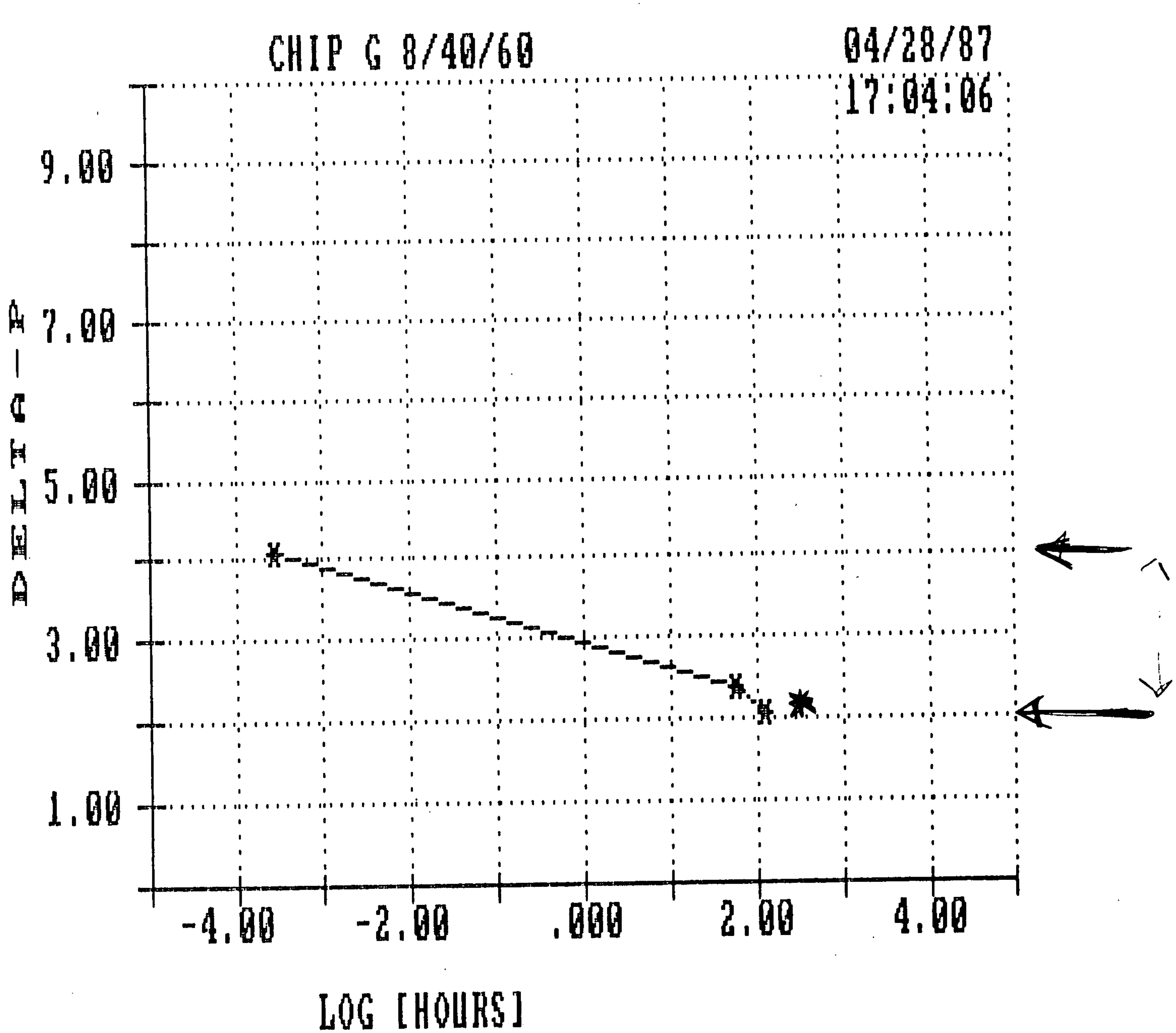
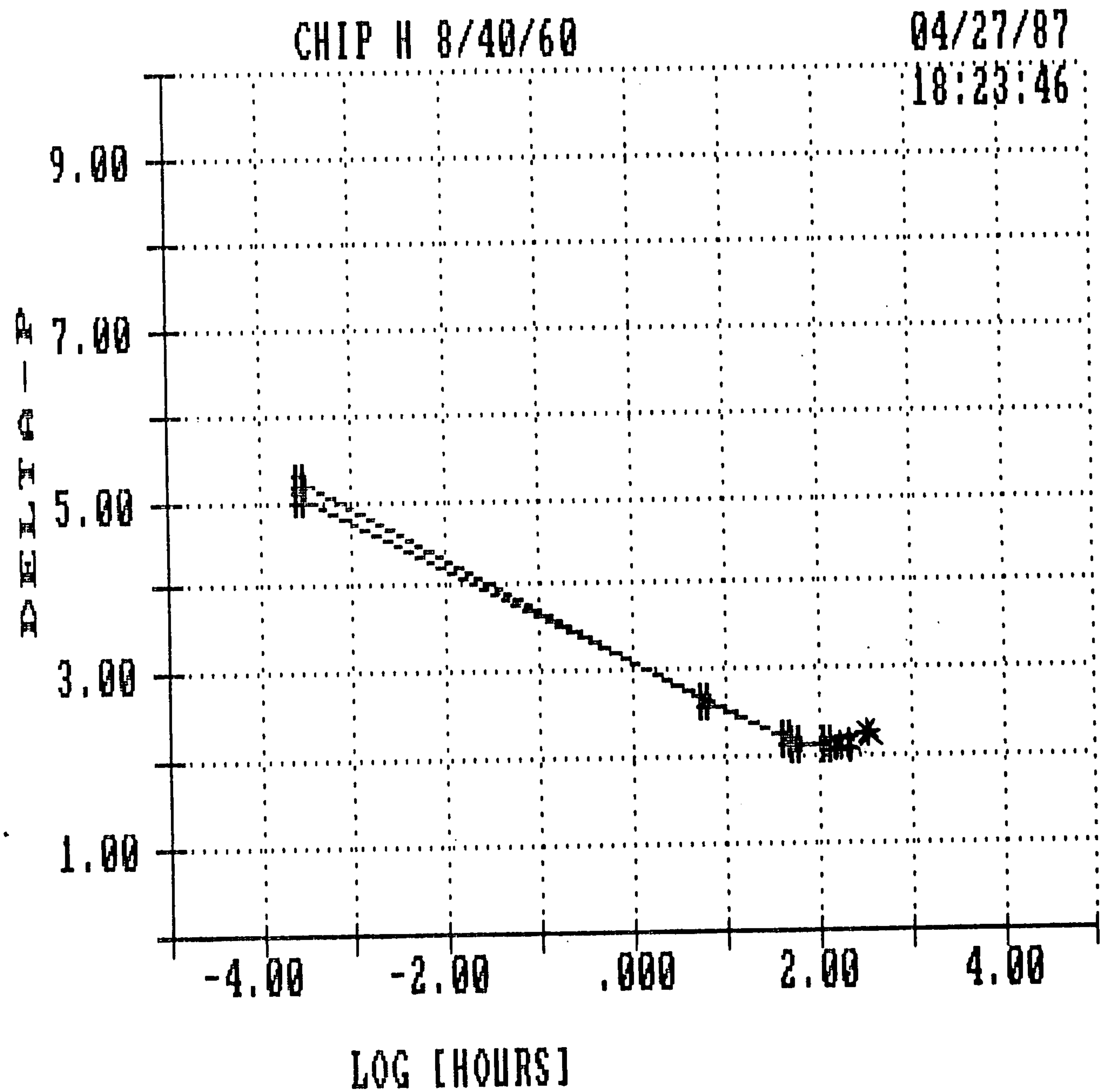

CHIP F 0/50/50
04/28/87
16:49:03
27.0
21.0
15.0
9.00
3.00
DELTA - A
-4.00
-2.00
.000
2.00
4.00
LOG [HOURS]

Figure 6



CHIP G 8/40/60
04/28/87
17:04:06
DELTA-P
9.00
7.00
5.00
3.00
1.00
-4.00
-2.00
.000
2.00
4.00
LOG [HOURS]

Figure 9



CHIP H 8/40/60
04/27/87
18:23:46
DELTA - A
9.00
7.00
5.00
3.00
1.00
-4.00
-2.00
.000
2.00
4.00
LOG [HOURS]

KRYSALIS CONFIDENTIAL

TO: Joe Evans DATE: April 30, 1987

FROM: Michael Cordoba

SUBJECT: LTF ON 8/40/60 AS A FUNCTION OF FREQUENCY

++
fat2.txt

Introduction-

In last wednesday's meeting there was some question as to whether the fatigue rate of Delta-P is frequency independent. In order to look at this issue we stressed two chips of lot "C" (i.e. 8/40/60 material) at two different frequencies at 10 KHz and at 1 MHz.

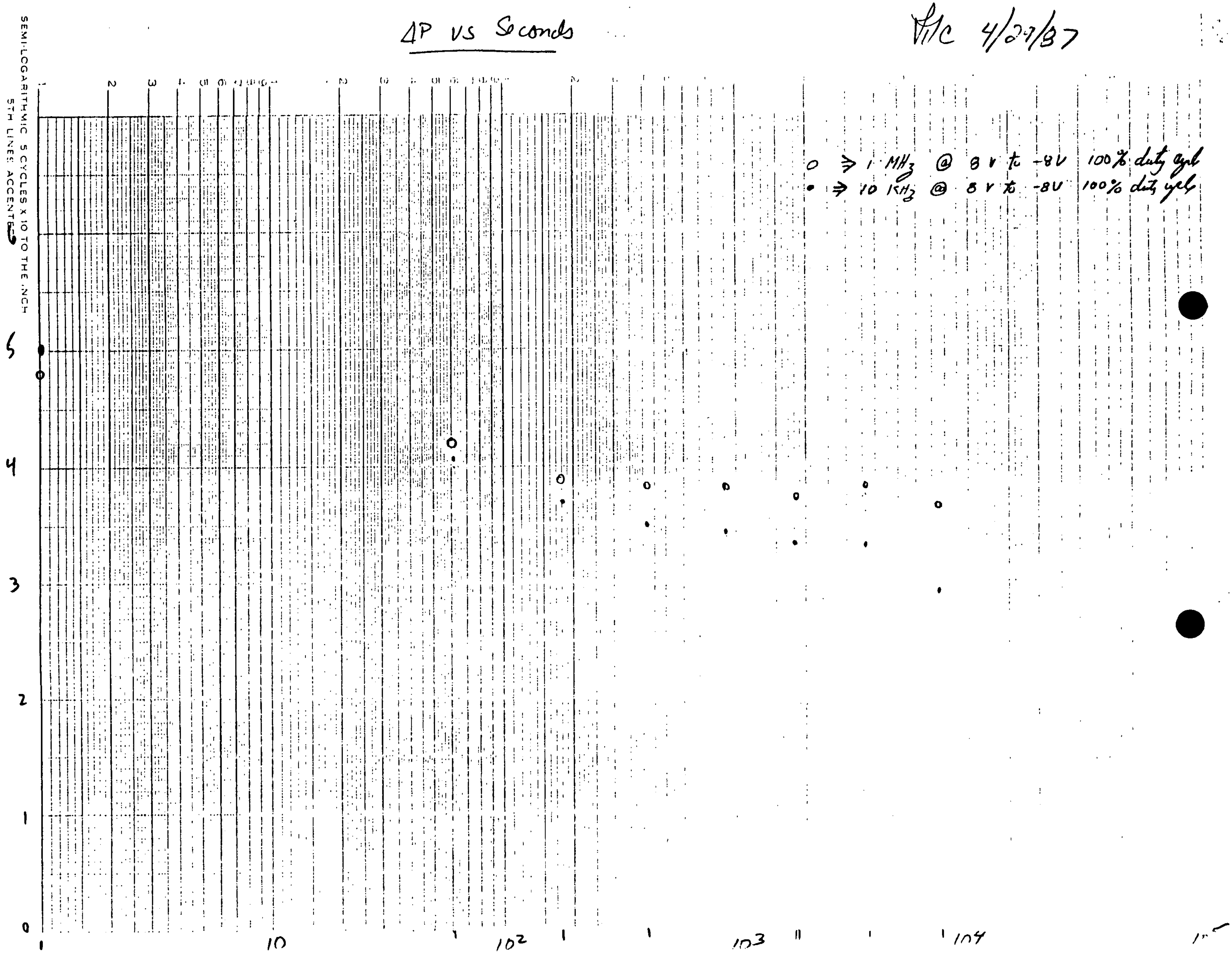
Anita measured the Delta-P at the following times specified in table 1 below. The data is graphed in figure 1 and it is also graphed with ranges in figure 2.

table 1

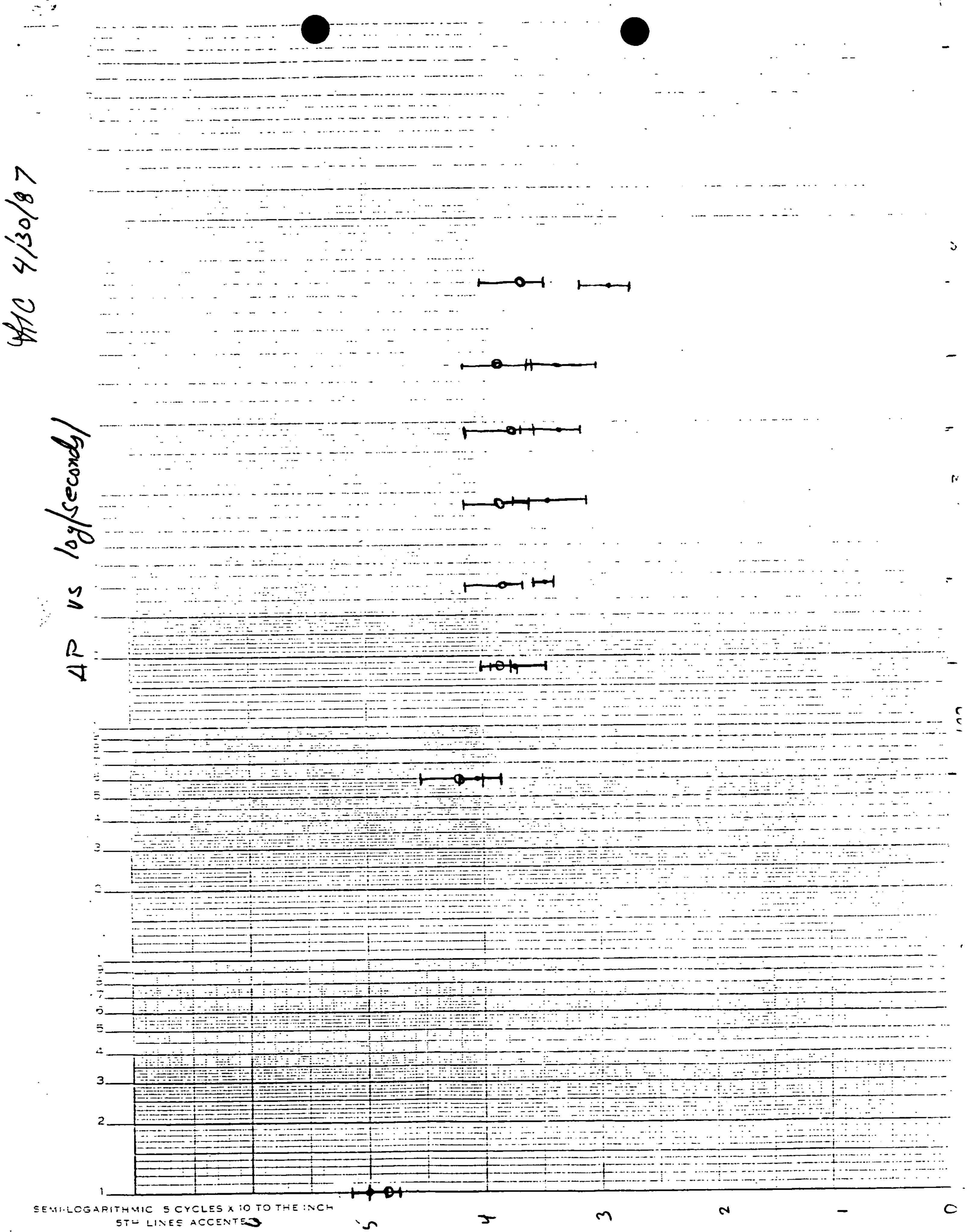
time between stresses	10 KHz Delta-P	1 MHz Delta-P
1 sec	5.00	4.84
1 min	4.06	4.21
2 min	3.70	3.88
4 min	3.47	3.82
8 min	3.44	3.85
16 min	3.32	3.74
32 min	3.38	3.84
64 min	2.91	3.69
128 min	3.11	3.75

Conclusions -

The first thing to notice from figure 1 is that after an initial fast decay, the fatigue rate is relatively flat. One can conclude that fatigue rate is not a strong "obvious" function of frequency at less than 1 hour of stress time. However, it still may be a function of frequency at later times, notice in figures 1 and 2 that the points seem to spread further apart as time goes on.



ΔP vs Seconds
Vilc 4/27/87
o ⇒ 1 MHz @ 8 V to -8V 100% duty cycle
• ⇒ 10 KHz @ 8 V to -8V 100% duty cycle
SEMI-LOGARITHMIC 5 CYCLES X 10 TO THE INCH
5TH LINES ACCENTED
0
1
2
3
4
5
1
10
10^2
10^3
10^4



SEMI-LOGARITHMIC 5 CYCLES X 10 TO THE INCH
5TH LINES ACCENTED

KRYSALIS CONFIDENTIAL

9

DATE: April 30, 1987

TO: Joe Evans

FROM: Michael Cordoba

SUBJECT: Transistor PCM Parameters with & without FES

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TRANFES.txt

Introduction-

This a quick look to see that transistor parameters are not effected by the " new " materials we are integrating with silicon technology. I measured the VT and Beta of two Orbit wafers, one with and one without our materials (refer to table 1). The structures measured where 30/30 transistors on Orbit PCM and 20/20 transistors on the Krysalis ECD512.

table

structure & location	silicon Orbit PCM		silicon & Kry materials Krysalis ECD512	
	Vt	Beta	Vt	Beta
n-ch center	1.03	41	.90	39
n-ch top	1.02	41	.91	40
p-ch center	-.92	14.5	-.92	12
p-ch top	-.96	14.6	-.97	13.2

note - units of Vt are volts and Beta is in uA/V^2

Conclusions -

Transistor threshold voltage and Beta are very similar for Orbit wafers with silicon technology and with our technology integrated with silicon.

10

KRYSALIS CONFIDENTIAL

TO: Joe Evans

DATE: May 14, 1987

FROM: Michael Cordoba

SUBJECT: LTF NEGATIVE DC STRESS

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nfat.txt

Introduction-

Wayne went to the American Ceramic Society Conference and spoke to David Payne about the " oxygen pumping " fatigue mechanism in $BatiO_3$ capacitors and about the elimination of the degradation by coating them (prevents exposure to atmospheric Oxygen).

With reference to this information Bill M. suggested that maybe the reason that a positive DC stress causes no degradation (with respect to the LTF system)is because of the biasing of the capacitor allows no oxygen to enter. He suggested a quick experiment with 8/40/60 using a negative DC bias, to see if there is degradation.

Results -

Chip C (i.e. lot 7069D, 8/40/60 with structure 1) was place on LTF for 1 sec, 15 minutes, 1.025 hrs. and 10.42 hours with a DC stress of - 8 volts. Virtually no fatigue was visible. Please refer to the attached results.

Conclusions and Suggestions -

Fatigue does not oocur with a DC stress and is independent of polarity. However, this still does not necessarily rule out the possibity of " oxygen pumping " causing fatigue in the capacitors that are AC stressed.

We should look at AC fatigue with top passivation. If fatigue is still present (at the same rate) than we can rule out " oxygen pumping " as a mechanism of fatigue.

MPLE # 3LNC41.P1 - 8/40/60 - 2.78E-4 HRS. (DC -8VOLTS)

CHIP NUMBER	HYSTE DELTA P(uC)	HYSTE Ps-Pr (uC)	PULSE DELTA P(uC)	PULSE Ps-Pr (uC)	Vc (V)	1/RatL
1	4.67	17.7	2.97	17.8	.92	1.167
2	5.07	17.7	2.89	17.5	.92	1.165
3	4.67	17.5	1.11	-7.0	.91	.843
4	5.47	17.6	3.58	18.0	1.00	1.200
5	5.47	17.3	3.17	17.9	.92	1.177
6	5.47	17.3	3.33	17.8	.95	1.187
7	5.07	16.9	3.67	17.8	.99	1.206
8	4.93	17.2	2.93	17.3	.99	1.169
9	5.60	16.8	2.91	17.3	.96	1.168
10	5.20	17.2	2.91	17.5	.96	1.167
11	4.53	17.5	3.33	17.8	.91	1.187
12	5.20	17.6	2.71	17.7	1.00	1.153
13	5.20	16.8	3.80	18.0	.93	1.211
14	4.67	17.3	3.09	17.7	.95	1.175
15	5.20	16.8	2.91	17.4	.95	1.167
MEAN	5.10	17.3	3.11	17.7	.95	1.176
3SIGMA	.0191	.865	.8427	.62	.08	.043

*PLE # 3LNC41.P2 - 8/40/60 - .25 HRS. (DC -8VOLTS)

CHIP NUMBER	HYSTE DELTA P(uC)	HYSTE Ps-Pr (uC)	PULSE DELTA P(uC)	PULSE Ps-Pr (uC)	Vc (V)	1/RatL
1	4.40	17.2	2.75	17.2	.96	1.160
2	4.67	17.3	2.73	17.0	.80	1.160
3	4.67	17.3	3.23	17.4	.85	1.185
4	4.40	17.2	2.73	17.0	.83	1.161
5	4.53	17.2	3.73	17.6	.80	1.212
6	4.40	16.8	3.14	17.2	.92	1.183
7	5.20	16.4	3.26	17.0	.92	1.192
8	4.80	16.8	2.69	16.7	.91	1.161
9	4.67	17.1	2.82	16.7	.99	1.169
10	5.20	16.8	3.29	17.2	1.00	1.191
11	4.93	17.2	2.53	16.9	.92	1.150
12	4.40	17.2	2.76	17.4	.83	1.158
13	4.67	17.3	3.73	17.5	.84	1.213
14	4.40	17.2	3.44	17.5	.96	1.197
15	4.40	17.2	2.61	16.9	.91	1.155
MEAN	4.63	17.1	3.01	17.1	.89	1.176
3SIGMA	.0093	.556	*****	.74	.17	.053

1PLE # 3LNC41.P3 - 8/40/60 - 1.025 HRS. (DC -8VOLTS)

CHIP NUMBER	HYSTE DELTA P(uC)	HYSTE Ps-Pr (uC)	PULSE DELTA P(uC)	PULSE Ps-Pr (uC)	Vc (V)	1/RatL
1	4.27	16.7	2.66	16.6	.88	1.161
2	4.67	16.7	3.13	16.9	.95	1.185
3	4.80	16.6	2.62	16.4	.92	1.159
4	4.67	16.8	2.88	16.7	.96	1.173
5	4.87	16.5	2.64	16.3	.92	1.162
6	5.00	16.7	2.94	16.6	1.01	1.177
7	5.20	15.3	3.40	16.0	1.01	1.212
8	4.87	16.2	2.76	16.2	1.01	1.171
9	4.93	16.4	2.75	16.5	1.03	1.167
10	5.00	16.3	2.56	16.6	1.01	1.154
11	5.27	16.1	2.49	16.4	.95	1.152
12	4.80	16.6	2.93	16.7	.92	1.175
13	4.47	16.8	3.69	17.0	.88	1.217
14	4.73	16.2	2.47	16.4	.95	1.150
15	5.87	16.4	3.99	16.7	1.09	1.238
MEAN	4.87	16.5	2.88	16.5	.96	1.174
3SIGMA	.0059	.644	*****	.54	.14	.058

PLE # 3LNC41.P5 - 8/40/60 - 10.42 HRS. (DC -8VOLTS)

CHIP NUMBER	HYSTE DELTA P(uC)	HYSTE Ps-Pr (uC)	PULSE DELTA P(uC)	PULSE Ps-Pr (uC)	Vc (V)	1/RatL
1	4.67	17.1	2.68	16.9	.96	1.158
2	4.60	17.1	2.84	16.9	.96	1.167
3	4.80	16.9	2.76	16.8	.96	1.164
4	5.27	16.5	3.69	17.4	.96	1.212
5	4.73	17.0	2.70	16.7	.96	1.162
6	5.13	17.1	2.94	17.2	.96	1.171
7	4.67	16.3	2.65	16.0	1.04	1.165
8	5.53	16.3	2.86	16.6	1.04	1.172
9	5.40	16.5	3.63	17.2	.96	1.211
10	4.80	17.1	3.09	17.1	.96	1.180
11	5.60	16.6	3.78	17.4	1.04	1.217
12	4.80	17.0	3.22	17.2	.96	1.188
13	4.80	17.0	2.60	16.9	.97	1.154
14	5.27	16.5	3.36	17.2	.96	1.195
15	5.93	16.2	3.46	16.9	1.12	1.205
MEAN	5.04	16.8	3.07	17.0	.98	1.181
3SIGMA	.0348	.869	*****	.66	.10	.056

KRYSALIS CONFIDENTIAL

TO: Joe Evans

DATE: ~~April 30~~ May 19, 1987

FROM: Michael Cordoba

SUBJECT: LTF May 15 Update

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fat.may

Introduction-

The latest results of LTF are available and show that 0/50/50 may be the material of choice! We are now extracting Pulse Delta-P and 1/RATL or LTAR as Rich likes to call it. The latest data in plots is for up to 678.1 hours. The plots presented are for the +/- 8 V AC pulse since that is the worst case condition.

Figures -

Figure 1 - Hysteresis Delta-P as a function of log time for the varios compositions with AC stress.

Figure 2 - Same as figure 1 except Pulse Delta-P.

Figure 3 - LTAR as a function of log time with varios compositions.

Figure 4 - LTAR as a function of temperature for 0/50/50.

Figure 5 - Pulse Delta-P as a function of temperature for 0/50/50.

Figure 6 - Hysteresis Delta-P as a function of log time for 8/40/60D.

Figure 7 - Hysteresis Delta-P as a function of log time for 8/40/60C.

Figure 8 - Hysteresis Delta-P as a function of log time for 3/40/60A.

Figure 9 - Hysteresis Delta-P as a function of log time for 0/50/50B.

Figure 10 - Pulse Delta-P as a function of log time for 0/50/50B. Note that figure 9 and 10 are on same scale for comparison purposes.

Figure 11 - Pulse Delta-P as a function of log time for 8/40/60C.

Figure 12 - LTAR as a function of log time for 0/50/50.

Figure 13 - LTAR as a function of log time for 3/40/60A.

Figure 14 - LTAR as a function of log time for 8/40/60C.

Discussions -

Figures 1, 2, 3, 4 and 5 summarize the results of the LTF. Figure 1 shows the delta-P for Hysteresis and figure 2 shows the data for pulse delta-P. It appears that 0/50/50 is the best material to use, in terms of having the highest delta-P. Extrapolating to 11 years (10^5 hours) shows that the Delta-P is still above 1.5 uC/cm^2. Note that 8/40/60 appears to be the worst material we can use, it already has after 678.1 hours a pulse delta-P that is below 1 uC/cm^2.

LTAR for all materials appear to be rather flat (refer to figure 3), in fact LTAR is increasing for the 0/50/50 which is also good.

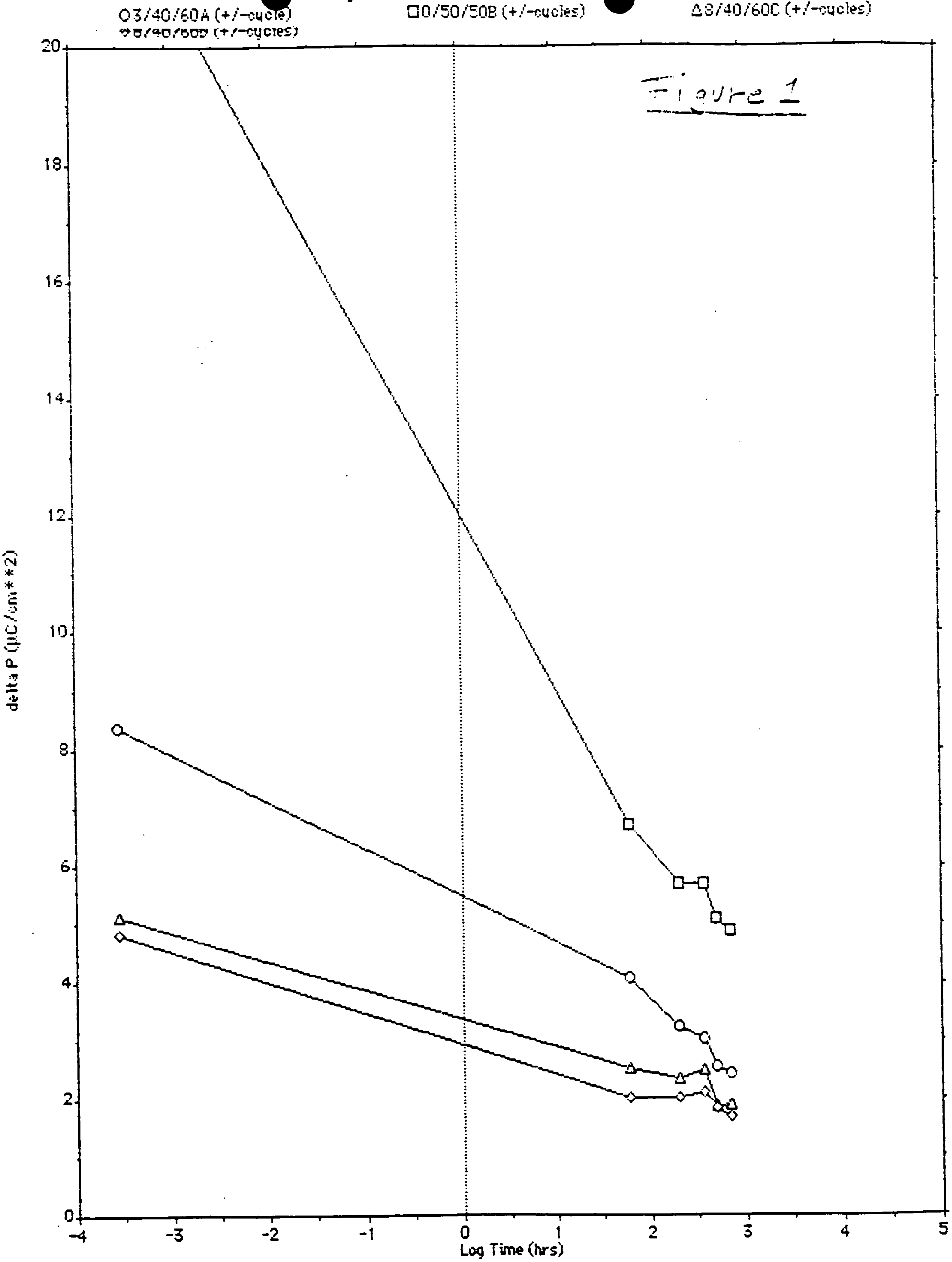
In order to give 0/50/50 some more serious consideration I ran a quick experiment to look at the variation of Delta-P and LTAR with respect to temperature. It appears that we loose about a factor of 2 of delta-P at high temperature (i.e. 150 C). Note also that LTAR decreases and seems to track with temperature the Delta-P change. Note that the part used for temperature testing was pre-stressed with +/- AC for 41 hours so that measuring the Delta-P at the varios temperatures would not fatigue it significantly.

Figure 9 and 10 is 0/50/50 data for hysteresis and Pulse Delta-P, respectively. This data shows the difference between hysteresis and pulse Delta-P decreases with stress time. This information is probably significant in the puzzle of understanding fatigue.

Conclusions -

To quote Nicholas in The Miko, " ... non-volatile RAM which will change the face of the computer industry for all time was still not available. Until now." And I think we may be there with 0/50/50 !!!! We need to look closely at more data and at its low temperature characteristics, but we are definitely close. I do not believe we will make it with 8/40/60.

Long Term Fatique Data (May 16, [illegible]87)



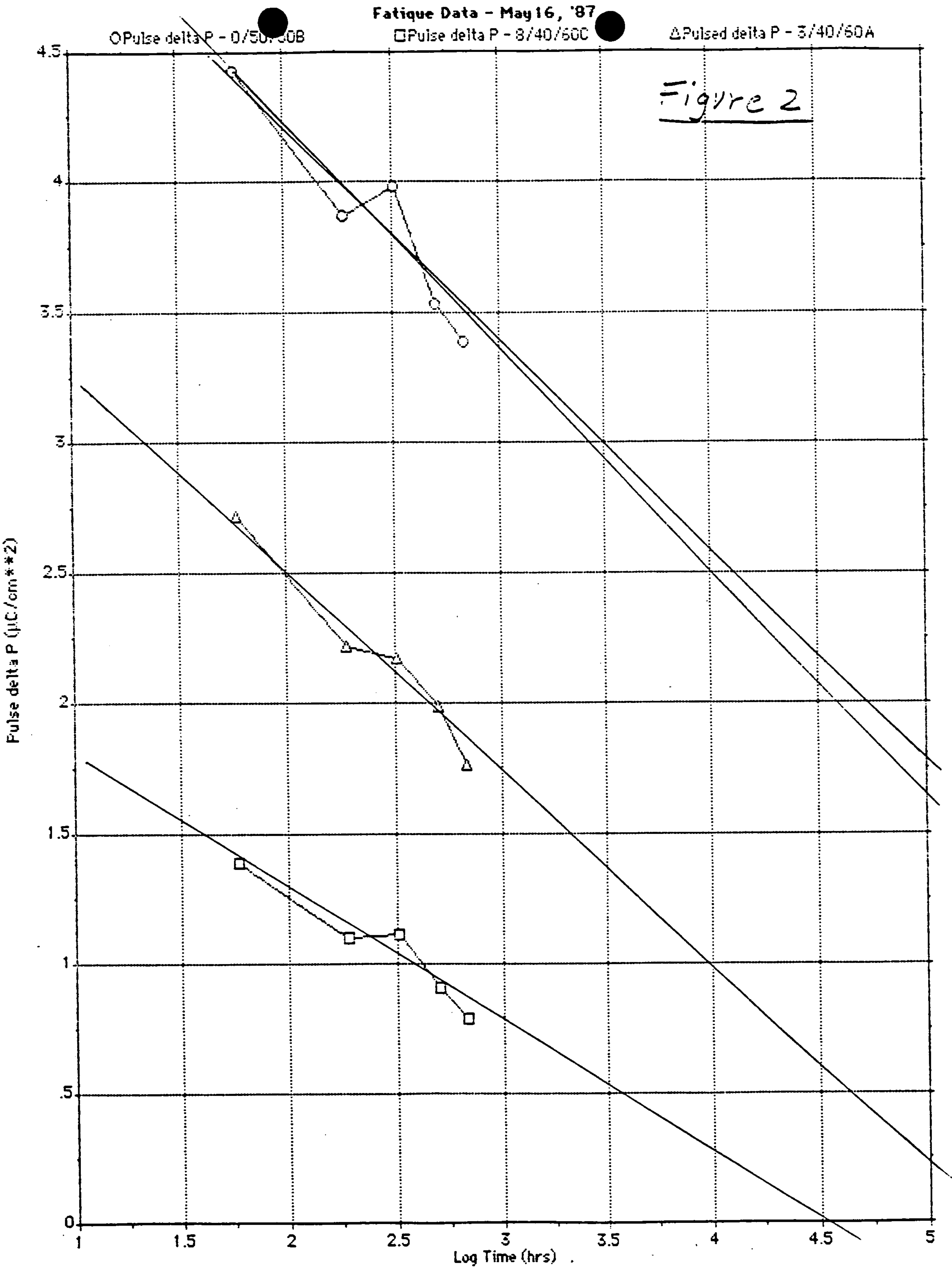
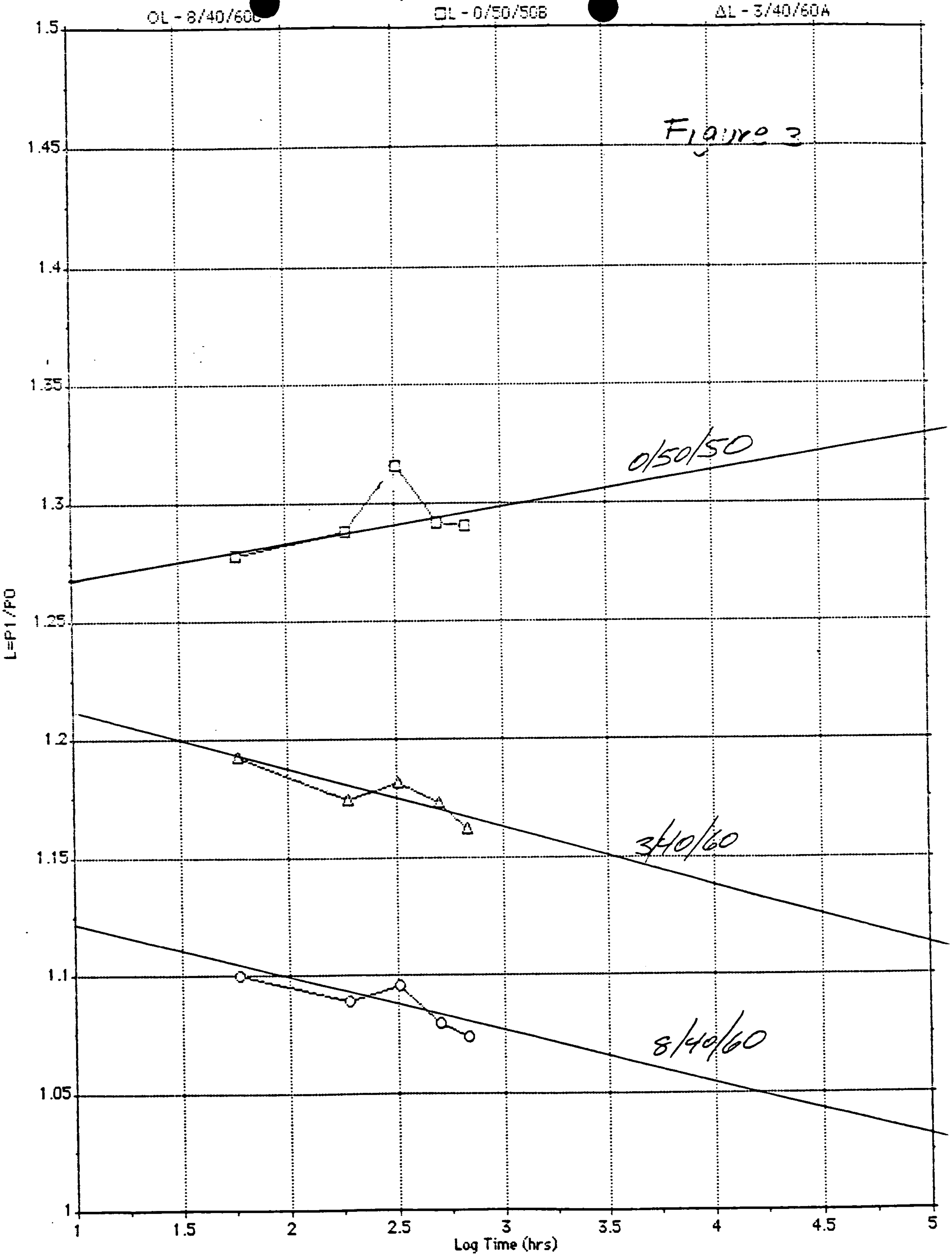
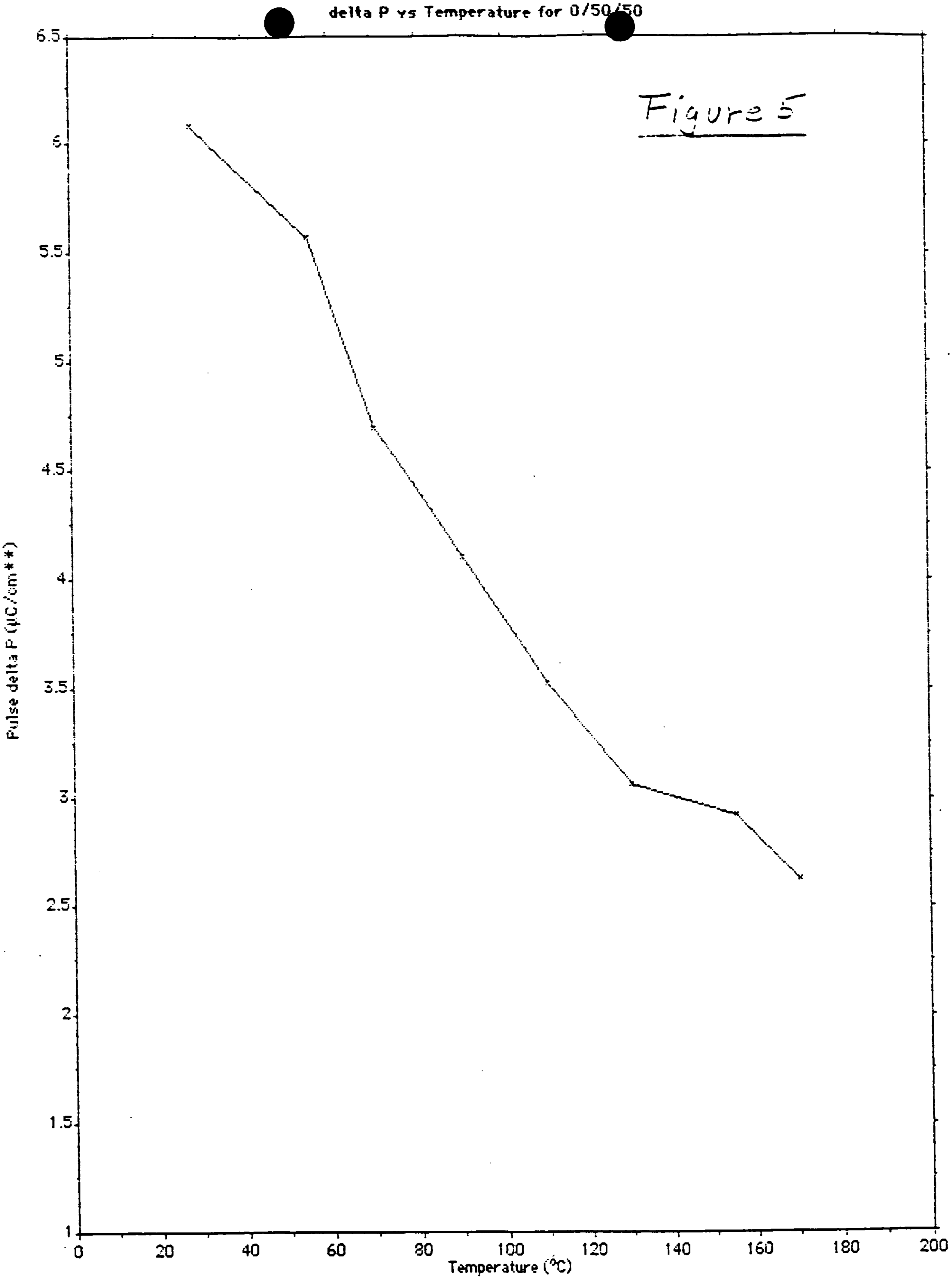

Fatique Data - May16, '87
○Pulse delta P - 0/5 0B
□Pulse delta P - 3/40/60C
△Pulsed delta P - 3/40/60A
Pulse delta P (µC/cm**2)
4.5
4
3.5
3
2.5
2
1.5
1
.5
0
1
1.5
2
2.5
3
3.5
4
4.5
5
Log Time (hrs)

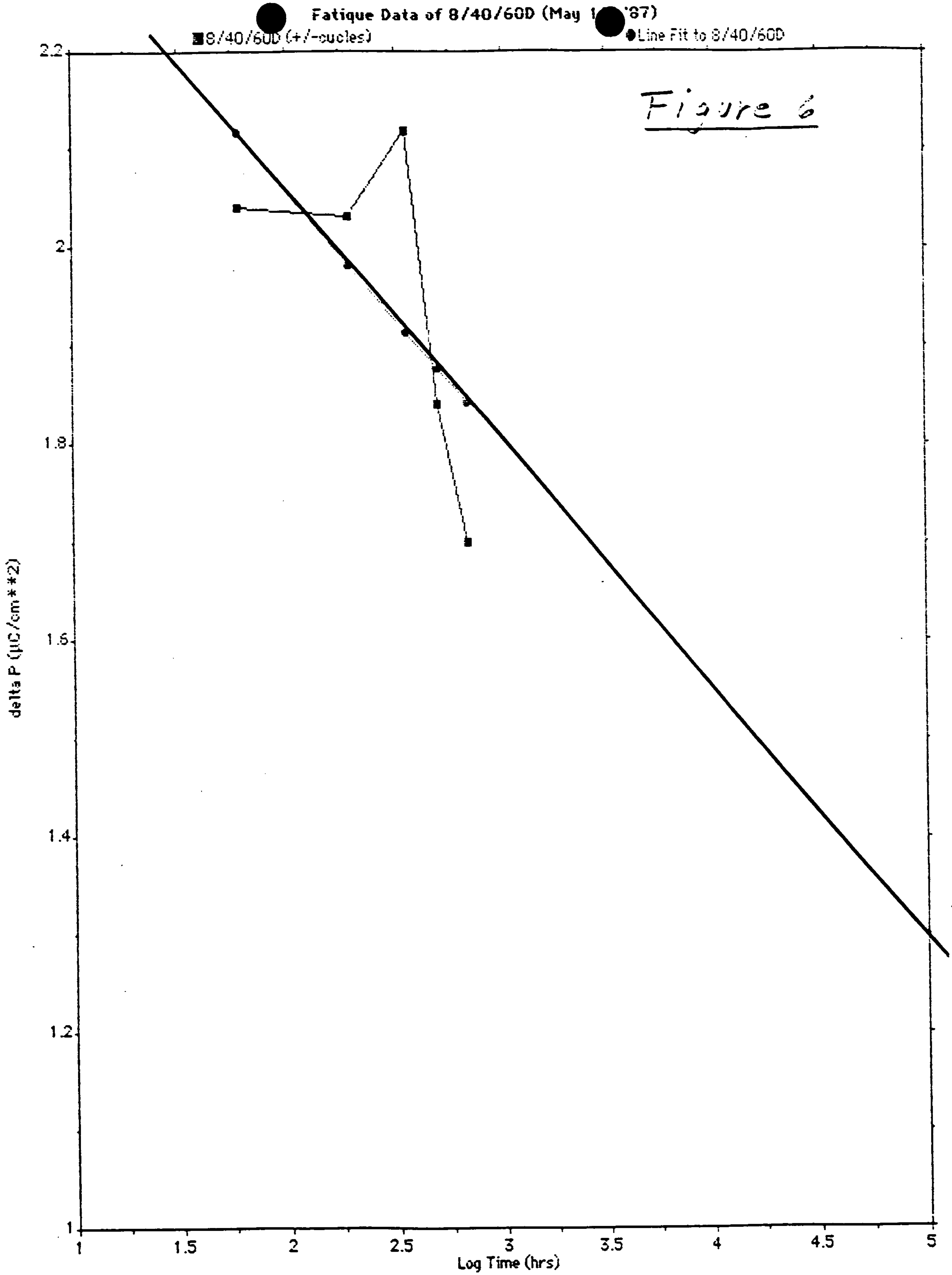
Figure 2

Fatique Data - May 16, 1987

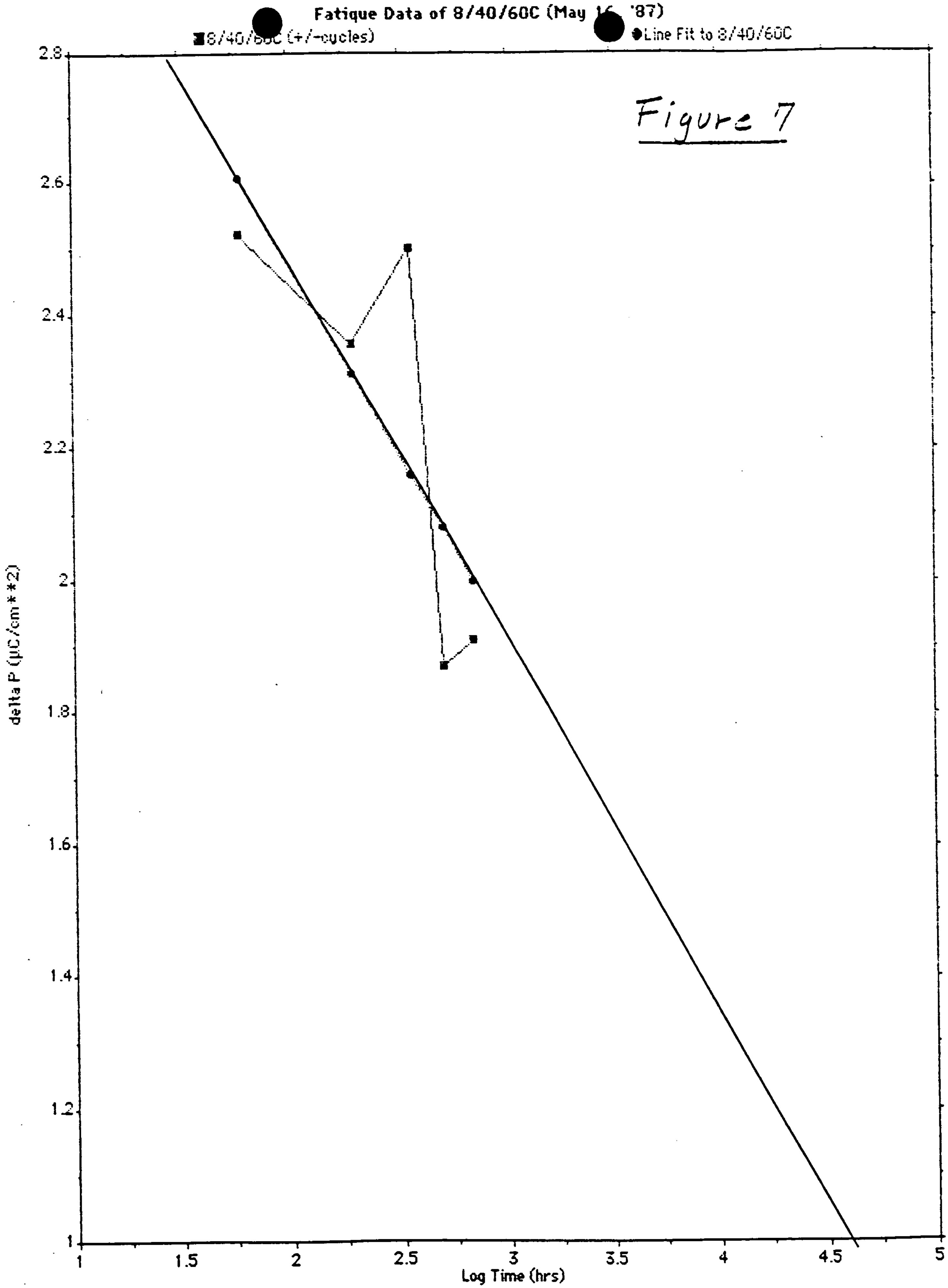


L vs Temperature for 0/50/50
Figure 4
L=P1/P0
1.35
1.3
1.25
1.2
1.15
1.1
1.05
1
0
20
40
60
80
100
120
140
160
180
200
Temperature (°C)

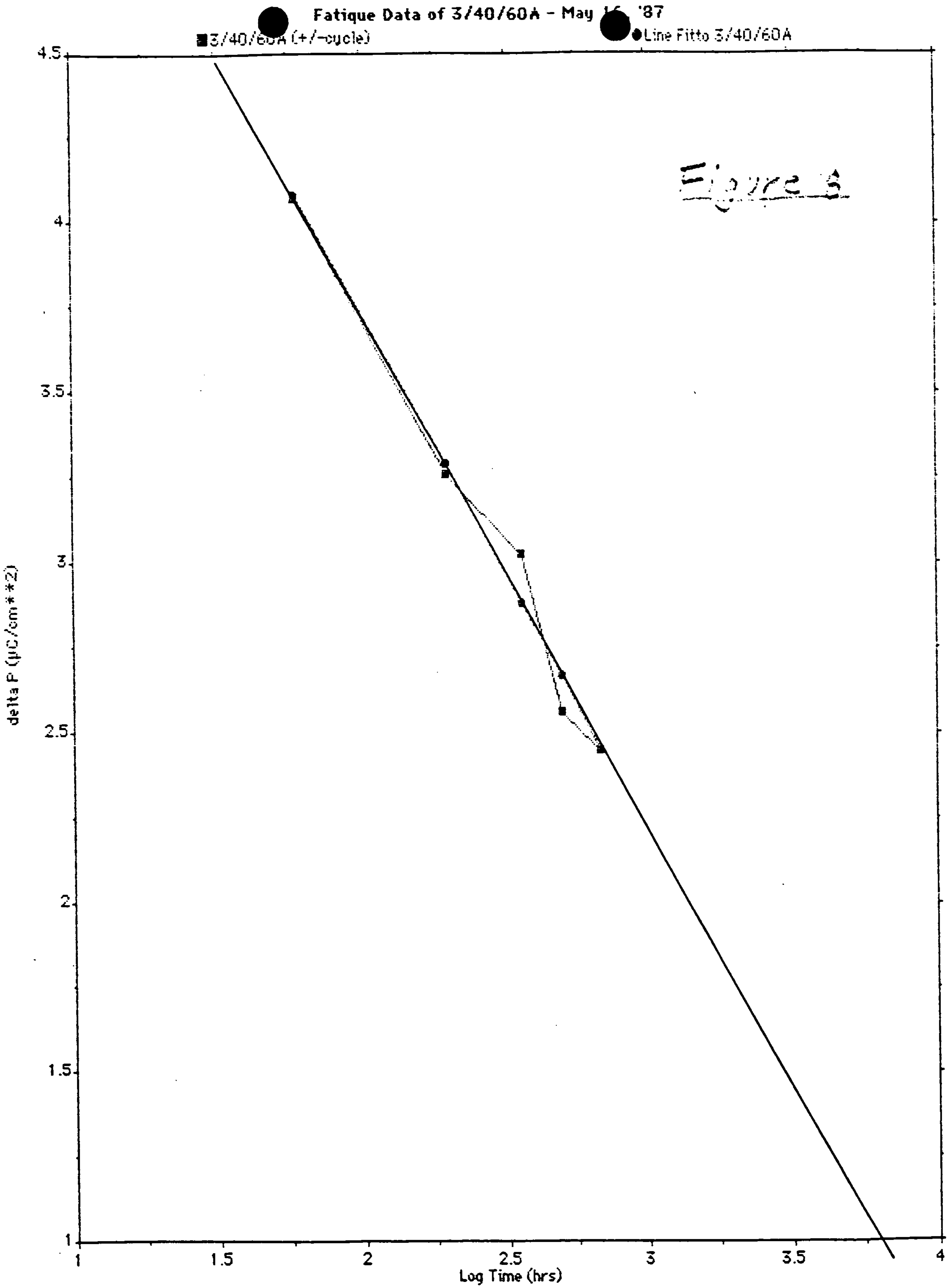

delta P vs Temperature for 0/50/50
Figure 5
Pulse delta P (µC/cm**)
Temperature (°C)
6.5
6
5.5
5
4.5
4
3.5
3
2.5
2
1.5
1
0
20
40
60
80
100
120
140
160
180
200

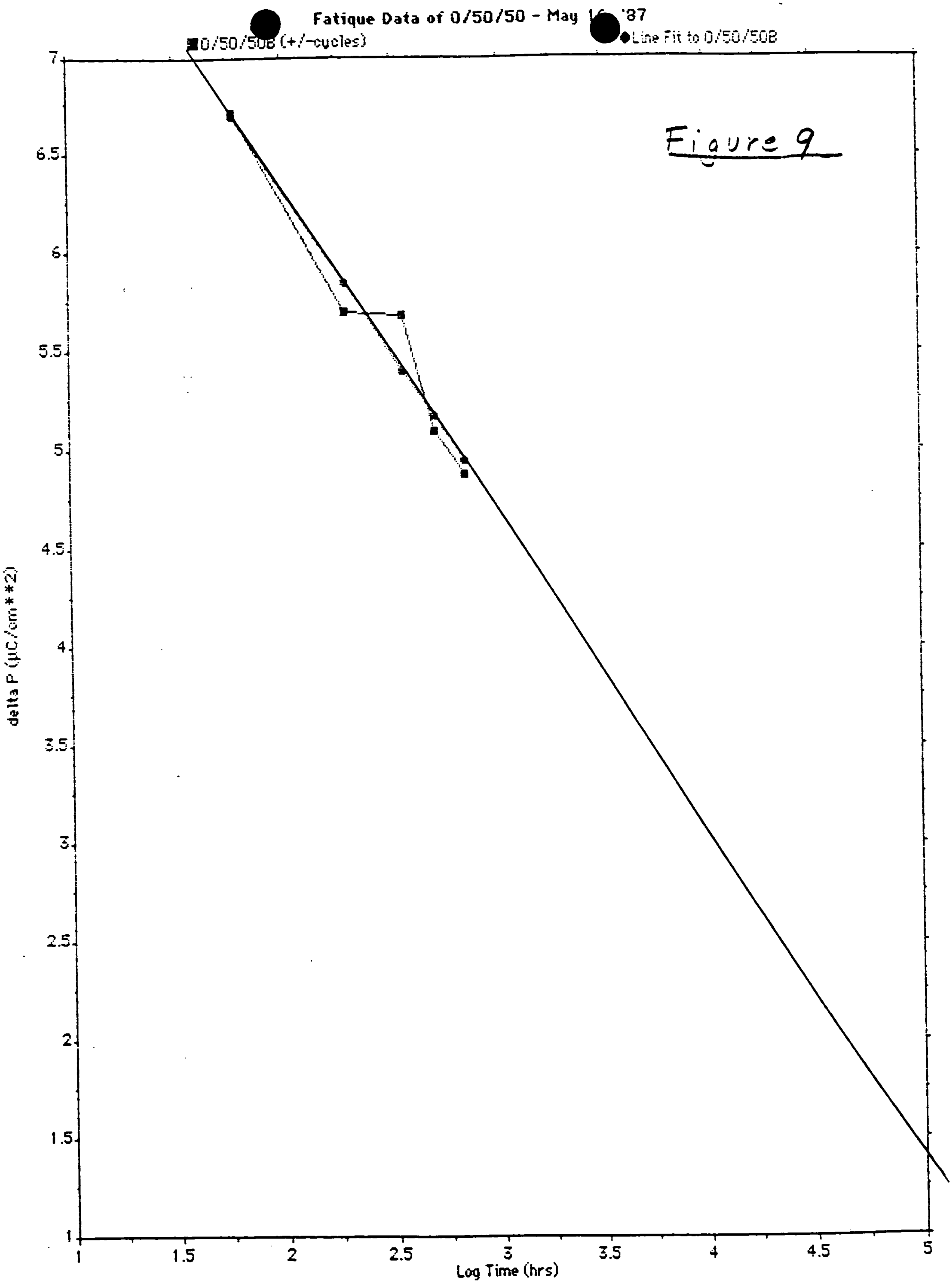


Fatique Data of 8/40/60D (May 1 '87)
8/40/60D (+/-cucles)
Line Fit to 8/40/60D
Figure 6
2.2
2
1.8
1.6
1.4
1.2
1
delta P (μC/cm**2)
1
1.5
2
2.5
3
3.5
4
4.5
5
Log Time (hrs)

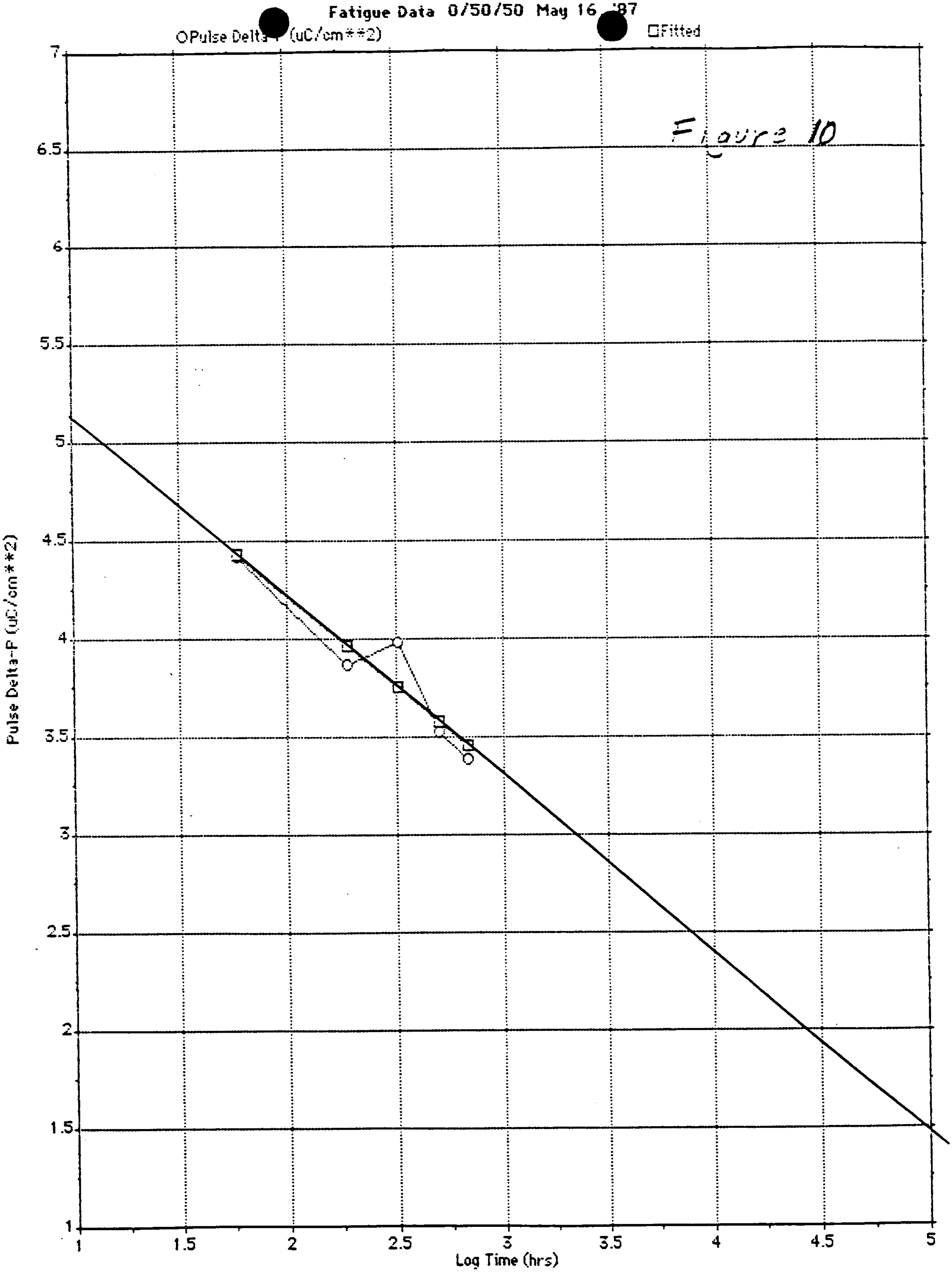


Fatique Data of 8/40/60C (May 16, '87)
8/40/60C (+/-cycles)
Line Fit to 8/40/60C
Figure 7
2.8
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
delta P (μC/cm**2)
1
1.5
2
2.5
3
3.5
4
4.5
5
Log Time (hrs)


Fatique Data of 3/40/60A - May '87
3/40/60A (+/-cycle)
Line Fitto 3/40/60A
Figure 3
delta P (μC/cm**2)
4.5
4
3.5
3
2.5
2
1.5
1
1.5
2
2.5
3
3.5
4
Log Time (hrs)

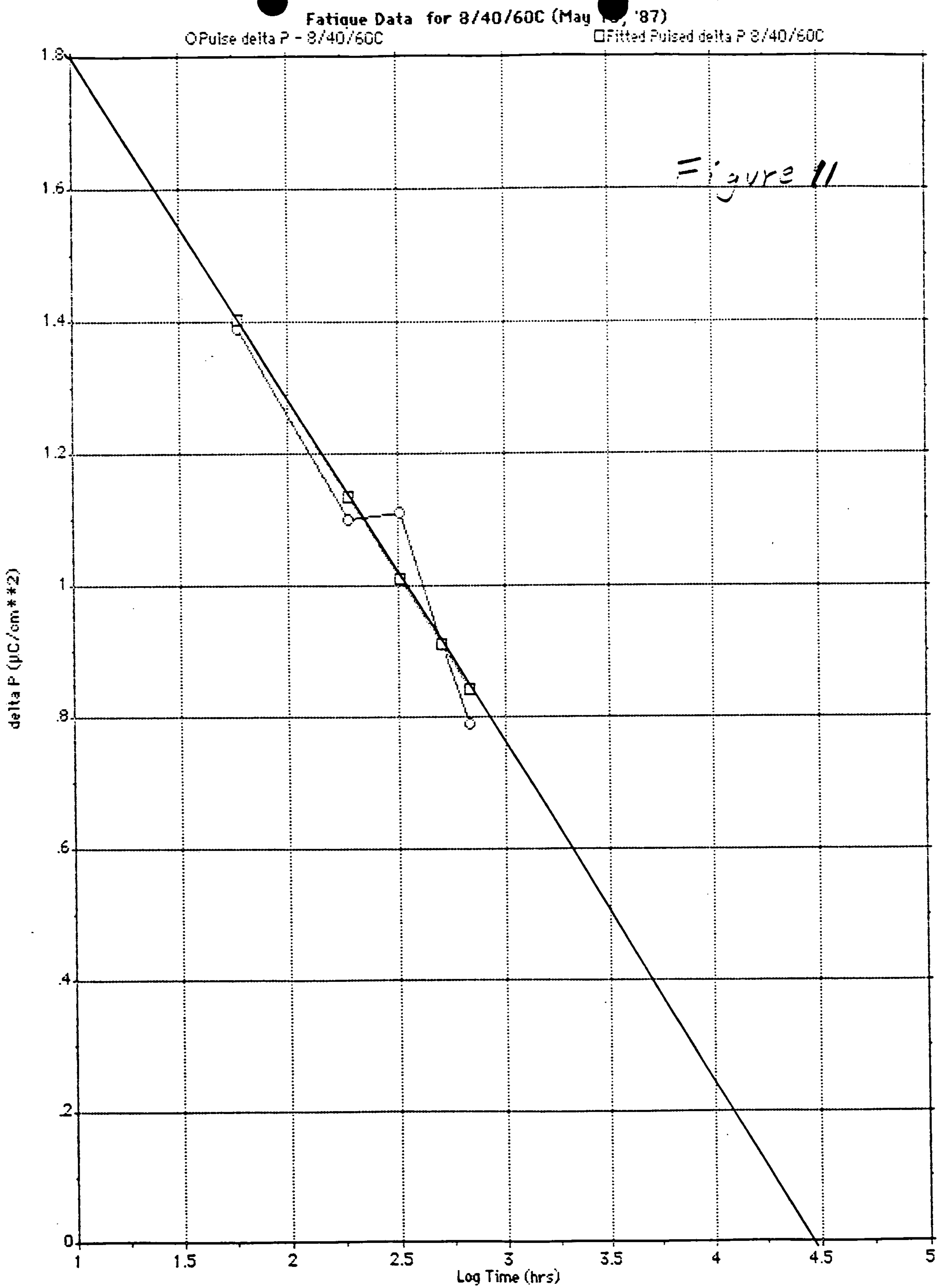


Fatique Data of 0/50/50 - May 16 '87
0/50/50B (+/-cycles)
Line Fit to 0/50/50B
Figure 9
delta P (μC/cm**2)
Log Time (hrs)
7
6.5
6
5.5
5
4.5
4
3.5
3
2.5
2
1.5
1
1
1.5
2
2.5
3
3.5
4
4.5
5

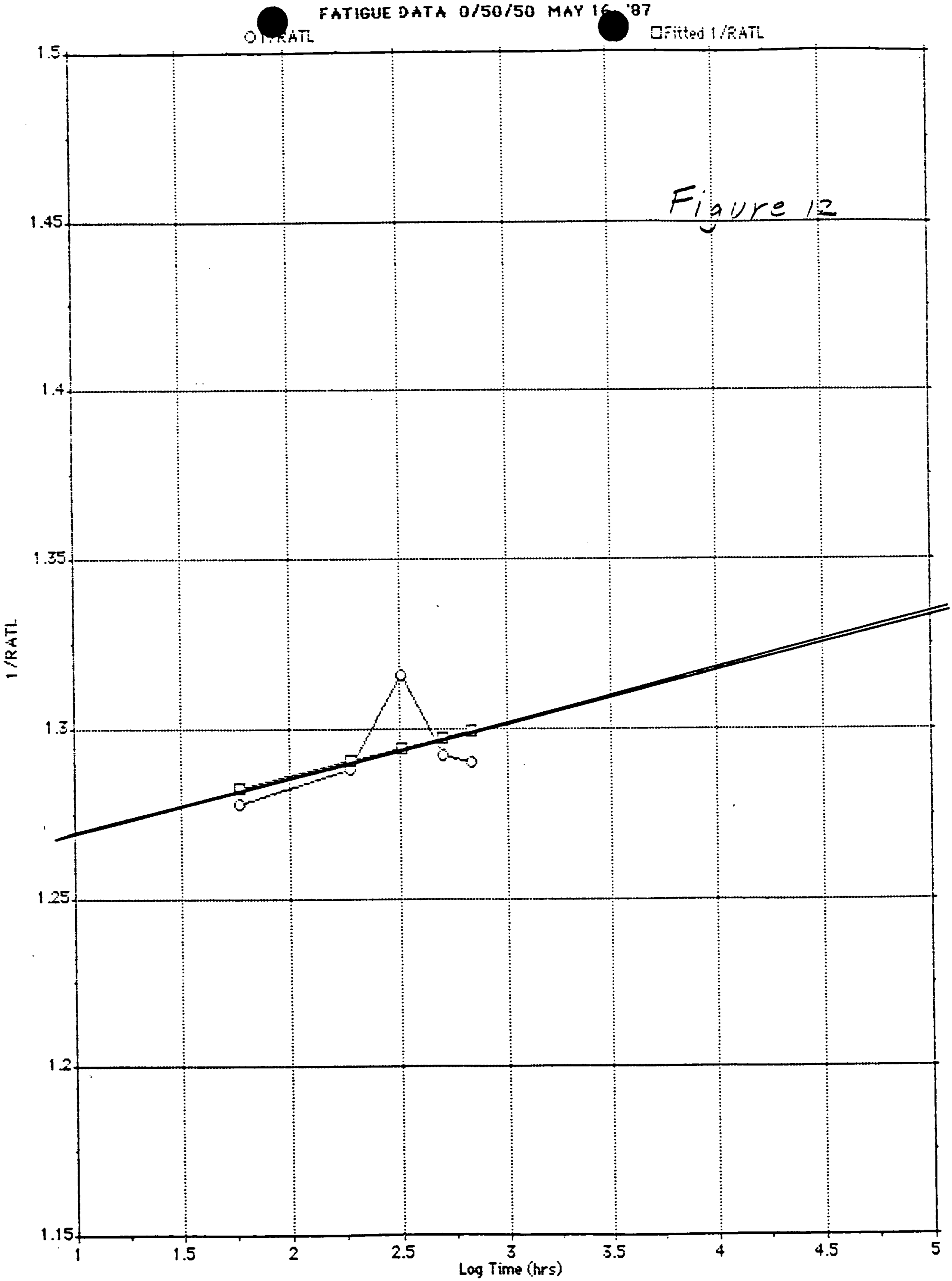


Fatigue Data 0/50/50 May 16, '87
Fitted
Pulse Delta-P (uC/cm**2)
Log Time (hrs)
7
6.5
6
5.5
5
4.5
4
3.5
3
2.5
2
1.5
1
1
1.5
2
2.5
3
3.5
4
4.5
5

Figure 10



Fatique Data for 8/40/60C (May 1?, '87)
OPulse delta P - 8/40/60C
□Fitted Pulsed delta P 8/40/60C
Figure 11
delta P (μC/cm**2)
1.8
1.6
1.4
1.2
1
.8
.6
.4
.2
0
1
1.5
2
2.5
3
3.5
4
4.5
5
Log Time (hrs)



FATIGUE DATA 0/50/50 MAY 16, '87
O 1/RATL
□Fitted 1/RATL
Figure 12
1.5
1.45
1.4
1.35
1.3
1.25
1.2
1.15
1 /RATL
1
1.5
2
2.5
3
3.5
4
4.5
5
Log Time (hrs)

Fatigue Data 3/40/60 A MAY 16, '87

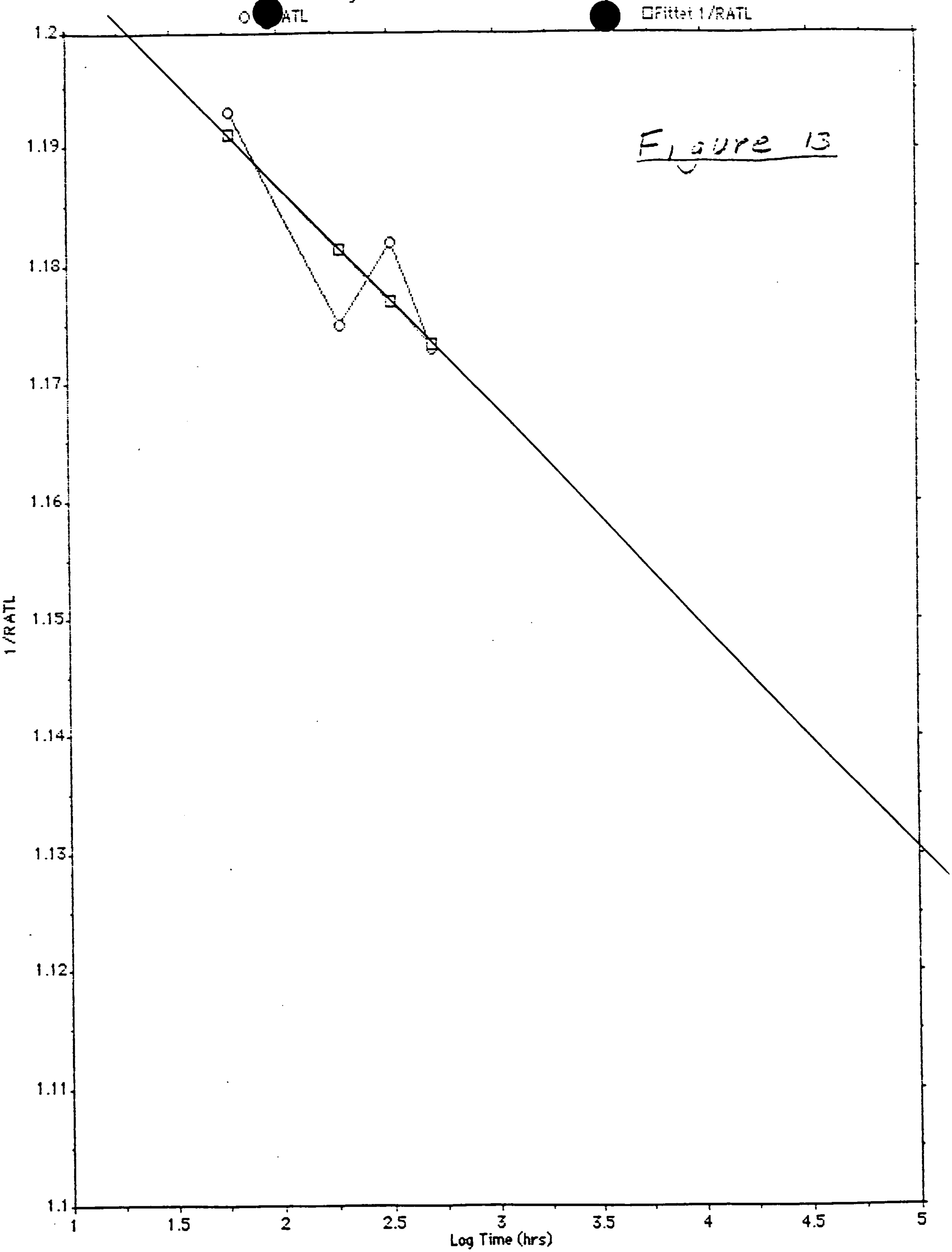


Figure 13

Fatique Data for 8/40/60C - May [illegible], '87

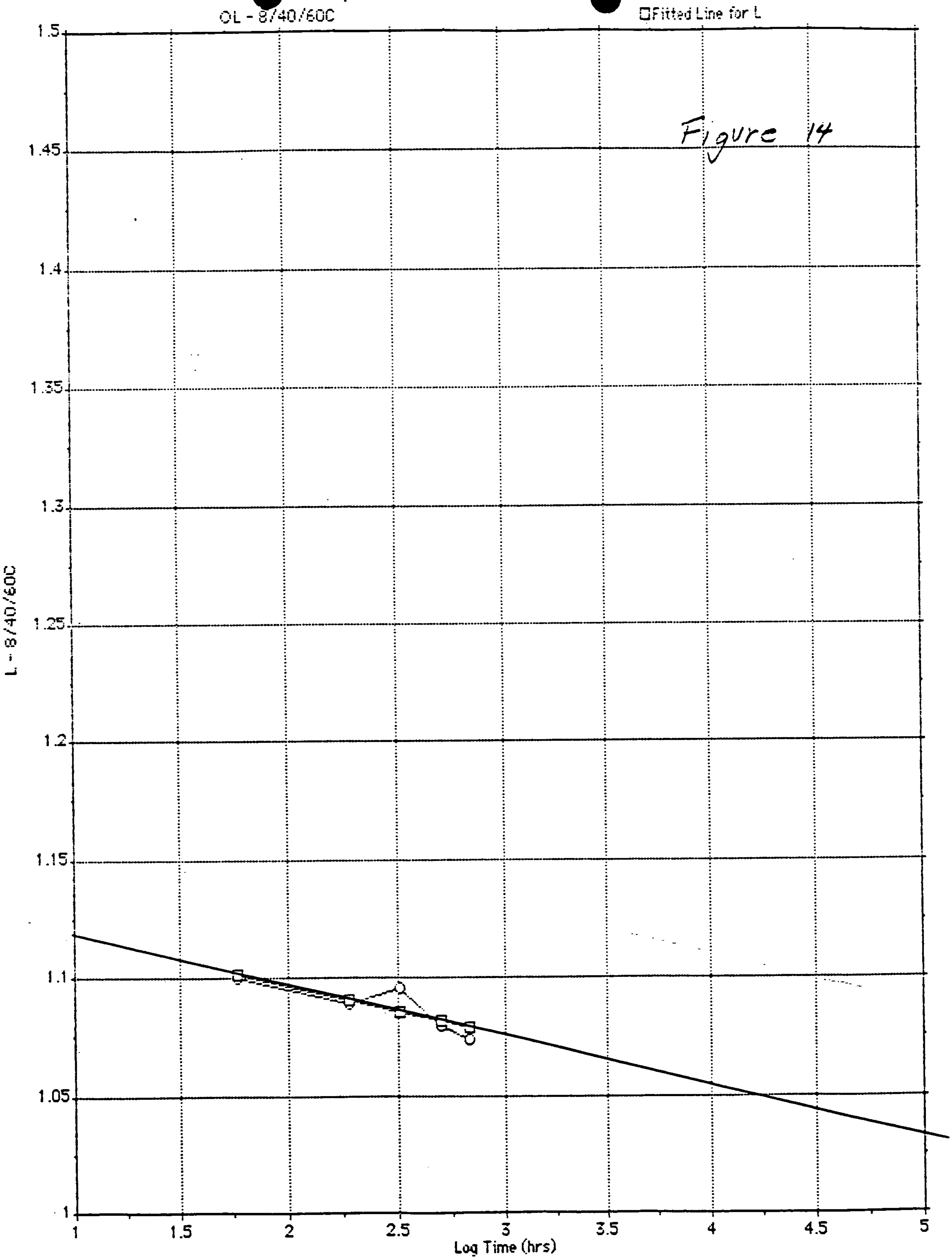


Figure 14

B/ //

12

TEST REPORT KRYSALIS CORPORATION

TO: Joe Evans DATE: May 21, 1987

FROM: Michael Cordoba

SUBJECT: Multi-coat and Thin-coat Compositions

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composit.txt

Introduction-

This experiment looked at the polarization of multi-coat and thin-coat compositions on Fat1 structures. Also a TD01 CMOS wafer (sample #1 in Table 1) was tested.

Results -

The TD01 wafer, was an experiment to determine whether the protective Nitride can be removed earlier in the process. The nitride was removed pre-Bel. The measurements indicated that the contacts were not opened on this wafer, so no measurements could be made.

The buffer layer sample 7121A with 1 coat 8/40/60 and 6 coats 3/40/60 and 1 coat 8/40/60 looked good.

All the thin coat material (i.e 4 coats instead of 8) except for 7125E (8/40/60) were leaky.

Conclusions and Recommendations -

It appears that of all the thin layer compositions, the 8/40/60 was the only layer that was not leaky. I recommend that we package some of the thin 8/40/60 material and place it on LTF, as well as the buffer layer sample.

We should probably manufacture a buffer layer sample of 1 coat 8/40/60, 6 coats 0/50/50 and 1 coat 8/40/60. And place it on LTF and determine if it has an effect on the slope of fatigue as a function of log time.

Table 2

TEST FILM TRAVELER   Krysalis Confidential   May 19, 1987

FILM ID	SUBSTRATE	BEL	TEL	BAKE	ANNEAL	DAY MADE
(1) 7117A	TD01 CMOS	B77-5	TD01	2@400	30@650inO2	04/27/87

G7110(8/40/60,+10);8cts;7 days old
NOTES:TD01 CMOS with nitride removed pre-BEL

FILM ID	SUBSTRATE	BEL	TEL	BAKE	ANNEAL	DAY MADE
(2) 7121A	1000Å TiO2	B79-1	Fat1	2@400	30@650inO2	05/01/87

G7110/7072(8/40/60,+10;3/40/60,+10);1/6cts;11/49 days old
NOTES:Buffer layer study;1x8/40/60,+10:6x3/40/60,+10:1x8/40/60,+10

FILM ID	SUBSTRATE	BEL	TEL	BAKE	ANNEAL	DAY MADE
(3) 7125C	Nitride	B80-1	Fat1	2@400	30@650inO2	05/05/87

G7022(0/50/50,+10);4cts;103 days old
NOTES:1/2 Std. FES thickness

FILM ID	SUBSTRATE	BEL	TEL	BAKE	ANNEAL	DAY MADE
4 7125D	Nitride	B80-3	Fat1	2@400	30@650inO2	05/05/87

G7072(3/40/60,+10);4cts;53 days old
NOTES:1/2 Std. FES thickness

FILM ID	SUBSTRATE	BEL	TEL	BAKE	ANNEAL	DAY MADE
(5) 7125E	Nitride	B80-4	Fat1	2@400	30@650inO2	05/05/87

G7110(8/40/60,+10);4cts;15 days old
NOTES:1/2 Std. FES thickness

FILM ID	SUBSTRATE	BEL	TEL	BAKE	ANNEAL	DAY MADE
7135C	ECD512A		512	2@400	30@650inO2	05/15/87

G7110(8/40/60,+10);8cts;25 days old
NOTES:CMOS ECD512A;alloy Al for 10min@400°C

5/19/87 ~~Did not measure 7135C [illegible]~~

Completed test on 7121A, 7125C, 7125D & 7125E.

7117A to be tested 5/20/87

SAMPLE # 4S21A1.P1 - TOP POSITION - BUFFER LAYER STUDY. - 5/19/87

INITL DELTA P	CAP (pF)	TAN DEL (%)	DELTA P (uC)	Ps-Pr (uC)	LOGICO DELTA P	LOGICO Ps-Pr (uC)	Vc (V)	LEAKAGE CURRENT
1.8	165	3.0	1.71	14.4	.61	14.3	.73	3.7E -11
-.0	0	***	.06	.0	.04	.0	.00	1.3E -11
2.0	169	3.4	1.84	14.4	.67	14.2	.80	3.5E -11
2.1	168	3.4	1.90	14.2	.74	14.2	.76	3.3E -11

SAMPLE # 4S21A1.P2 - CENTER POSITION - BUFFER LAYER STUDY - 5/19/87

INITL DELTA P	CAP (pF)	TAN DEL (%)	DELTA P (uC)	Ps-Pr (uC)	LOGICO DELTA P	LOGICO Ps-Pr (uC)	Vc (V)	LEAKAGE CURRENT
1.9	165	3.0	1.94	14.9	.71	14.7	.85	3.7E -11
2.4	167	3.5	2.07	14.8	.69	14.7	.93	3.7E -11
2.0	163	3.7	1.95	14.3	.67	14.3	.89	3.5E -11
3.4	164	3.5	1.96	14.4	.62	14.4	.87	3.4E -11

SAMPLE # 4S21A1.P3 - BOTTOM POSITION - BUFFER LAYER STUDY - 5/19/87

INITL DELTA P	CAP (pF)	TAN DEL (%)	DELTA P (uC)	Ps-Pr (uC)	LOGICO DELTA P	LOGICO Ps-Pr (uC)	Vc (V)	LEAKAGE CURRENT
1.1	167	2.5	1.13	14.9	.45	14.8	.51	3.9E -11
1.3	169	2.9	1.21	14.7	.42	14.7	.53	4.3E -11
-.0	1	***	.00	.1	.11	.0	.00	1.2E -11
2.1	169	2.9	1.15	14.9	.40	14.9	.60	3.6E -11

SAMPLE # 4S25C1.P1 - TOP POSITION - 1/2 STD FES - 5/19/87 (LEAKY)

INITL DELTA P	CAP (pF)	TAN DEL (%)	DELTA P (uC)	Ps-Pr (uC)	LOGICO DELTA P	LOGICO Ps-Pr (uC)	Vc (V)	LEAKAGE CURRENT
4.0	225	1.7	3.48	17.7	.98	17.3	.96	3.5E -3
3.6	216	1.9	6.24	17.6	1.23	17.1	1.04	3.5E -3
-.1	1	***	.03	.1	-.02	.1	.00	1.2E -11
3.6	245	***	10.32	18.5	3.69	17.7	1.20	3.5E -3

SAMPLE # 4S25D1.P2 - CENTER POSITION - 1/2 STD FES - 5/19/87

INITL DELTA P	CAP (pF)	TAN DEL (%)	DELTA P (uC)	Ps-Pr (uC)	LOGICO DELTA P	LOGICO Ps-Pr (uC)	Vc (V)	LEAKAGE CURRENT
3.8	219	1.6	3.32	17.2	.80	17.0	.88	3.5E -3
5.3	221	***	44.24	.1	-1.67	45.7	1.09	3.5E -3
4.6	***	***	-3.68	47.6	-3.69	47.4	.99	3.5E -3
4.2	218	1.7	6.35	18.1	1.22	17.7	1.05	3.5E -3

SAMPLE # 4S25C1.P3 - BOTTOM POSITION - 1/2 STD. FES - 5/19/87

INITL DELTA P	CAP (pF)	TAN DEL (%)	DELTA P (uC)	Ps-Pr (uC)	LOGICO DELTA P	LOGICO Ps-Pr (uC)	Vc (V)	LEAKAGE CURRENT
3.5	218	1.7	3.40	17.3	.96	16.9	.88	3.5E -3
3.7	220	***	28.93	5.5	18.38	8.2	1.20	3.5E -3
.0	1	***	-.03	.2	.05	.1	.00	2.2E -9
4.2	221	1.6	6.36	18.2	1.28	17.7	1.04	3.5E -3

SAMPLE # 4S25D1.P2 - TOP POSITION - 1/2 STD FES - 5/19/87

INITL DELTA P	CAP (pF)	TAN DEL (%)	DELTA P (uC)	Ps-Pr (uC)	LOGIC0 DELTA P	LOGIC0 Ps-Pr (uC)	Vc (V)	LEAKAGE CURRENT
10.4	204	2.6	2.26	15.2	.77	15.0	1.12	1.2E -6
10.4	184	1.5	1.90	14.1	.39	14.0	.72	3.0E -6
10.5	43	***	.85	5.0	.17	4.9	.56	9.3E -8
10.5	181	1.6	1.84	13.7	.51	13.6	.72	3.3E -6

SAMPLE # 4S25D1.P3 - CENTER POSITION - 1/2 STD. FES - 5/19/87

INITL DELTA P	CAP (pF)	TAN DEL (%)	DELTA P (uC)	Ps-Pr (uC)	LOGIC0 DELTA P	LOGIC0 Ps-Pr (uC)	Vc (V)	LEAKAGE CURRENT
3.2	200	2.2	2.02	17.1	.66	16.9	.72	3.5E -3
3.3	207	***	47.25	.0	-3.46	46.9	1.11	3.5E -3
6.5	213	2.8	3.17	18.1	.83	17.9	.76	5.8E -9
4.5	214	2.7	2.99	18.3	.85	18.0	.79	3.5E -3

SAMPLE # 4S25D1.P4 - BOTTOM POSITION - 1/2 STD FES - 5/19/87

INITL DELTA P	CAP (pF)	TAN DEL (%)	DELTA P (uC)	Ps-Pr (uC)	LOGIC0 DELTA P	LOGIC0 Ps-Pr (uC)	Vc (V)	LEAKAGE CURRENT
3.7	200	1.8	2.20	17.4	.72	17.2	.64	3.5E -3
5.6	221	2.5	4.01	18.7	.96	18.4	.72	3.5E -3
5.7	224	2.4	4.71	19.1	1.04	18.7	.79	3.5E -3
4.9	224	2.3	4.50	19.4	1.04	19.0	.84	3.5E -3

SAMPLE # 4S25E1.P1 - TOP POSITION - 1/2 STD FES - 5/19/87

INITL DELTA P	CAP (pF)	TAN DEL (%)	DELTA P (uC)	Ps-Pr (uC)	LOGICO DELTA P	LOGICO Ps-Pr (uC)	Vc (V)	LEAKAGE CURRENT
5.7	234	2.6	1.84	18.2	.90	18.0	.65	7.9E -10
-.0	1	***	.00	.1	-.03	.1	.00	1.3E -11
2.7	242	2.4	1.91	18.0	.71	17.9	.64	6.6E -11
5.8	236	2.7	1.70	17.9	.69	17.8	.75	7.0E -10

SAMPLE # 4S25E1.P2 - CENTER POSITION - 1/2 STD. FES - 5/19/87

INITL DELTA P	CAP (pF)	TAN DEL (%)	DELTA P (uC)	Ps-Pr (uC)	LOGICO DELTA P	LOGICO Ps-Pr (uC)	Vc (V)	LEAKAGE CURRENT
2.3	236	2.6	1.84	18.7	.77	18.5	.64	2.4E -10
7.1	230	2.6	1.80	18.1	.78	17.8	.72	2.2E -10
5.1	233	2.6	1.79	18.2	.63	18.0	.68	1.2E -10
2.5	236	2.6	1.76	18.4	.74	18.2	.64	2.0E -10

SAMPLE # 4S25E1.P3 - BOTTOM POSITION - 1/2 STD. FES - 5/19/87

INITL DELTA P	CAP (pF)	TAN DEL (%)	DELTA P (uC)	Ps-Pr (uC)	LOGICO DELTA P	LOGICO Ps-Pr (uC)	Vc (V)	LEAKAGE CURRENT
5.5	246	2.4	2.01	19.1	.84	18.9	.69	4.7E -11
5.4	241	2.5	1.82	18.5	.74	18.3	.72	4.3E -11
2.3	237	2.5	1.70	18.2	.67	18.0	.72	7.4E -11
4.3	243	2.4	1.89	18.7	.77	18.5	.64	4.8E -11

TEST REPORT KRYSALIS CORPORATION

TO: Joe Evans DATE: June 2, 1987

FROM: Michael Cordoba

SUBJECT: ECD512A Parametrics

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param.txt

Introduction-

This is a cursory look at ECD512a parametrics. Looking specifically at contact strings, transitor parametrics and ferroelectric properties.

Results -

In general the transitor parametrics looked good, however there were some variations of Vt across the wafer of 150 mV.

The Al-P+ resistance is 10 to 100 times higher than a wafer processed completely by Orbit, and also it varies a great deal from wafer to wafer and across the wafer. Al-N+ contact resistance looks good, as does the Al-Tel contact strings.

The ferroelectric properties are slimmer looped for both 0/50/50 wafer and the 8/40/60 wafer when compared to non-CMOS wafers. The Delta-P for 0/50/50 is 5-6 uC/cm**2 and 8-9 uC/cm**2 on two ECD512a wafers, when typically it is 20-30 uC/cm**2 (i.e. prefatigued) on non-CMOS wafers.

Conclusions and Recommendations -

Conduct experiments on improving the AL-P+ contact resistance.

Look into determining whether Nitride is lowering the value of the initial Delta-P of the CMOS wafers and whether this is detrimental or helpful with respect to fatigue rate.

May 1987

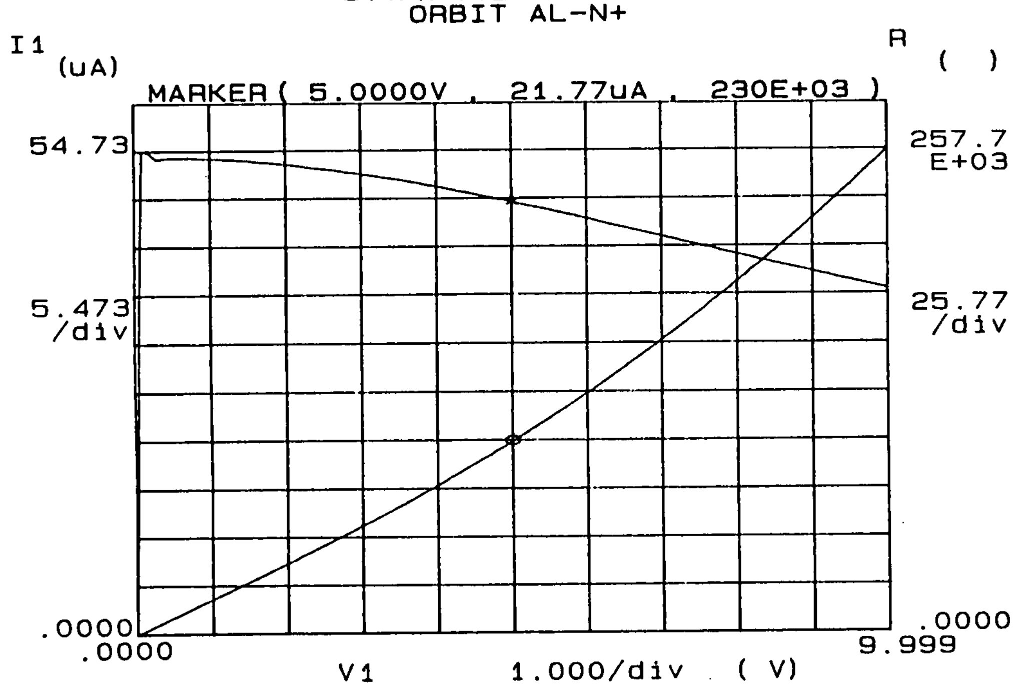
Orbit Contact Resistance

Al - N+

Al - P+

****** GRAPHICS PLOT ******

ORBIT AL-N+



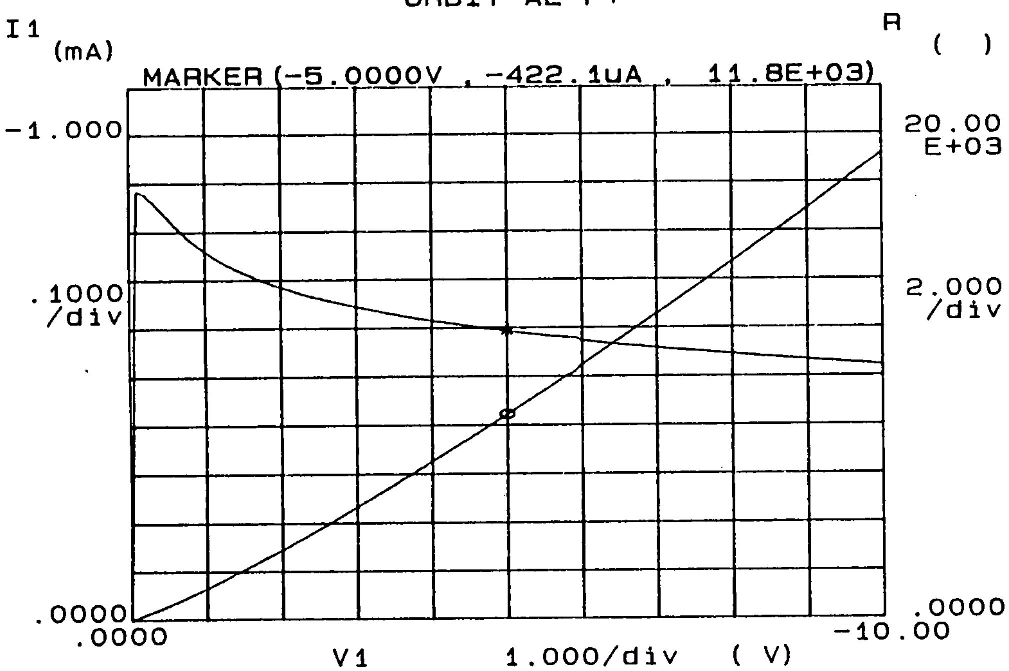
Variable1:
V1 -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V2 -Ch2 .0000V
V3 -Ch3 .0000V
V4 -Ch4 .0000V

R ( ) = V1/I1

****** GRAPHICS PLOT ******

ORBIT AL-P+



Variable1:
V1 -Ch1
Linear sweep
Start .0000V
Stop -10.000V
Step -.1000V

Constants:
V2 -Ch2 .0000V
V3 -Ch3 .0000V
V4 -Ch4 .0000V

R ( ) = V1/I1

Krysalis Confidential

Parametric Data

Date : May 26, 1987

Foundry : Orbit

Wafer ID: 7139A

Wafer Description: ECD512A 0/50/50

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Transistor Parametrics

N-ch:

Size	FLAT Location 1	CENTER Location 2	TOP Location 3
Vt (volts)	.875	.887	.891
Beta (uA/V²)	41.9	41.3	40.0

P-ch:

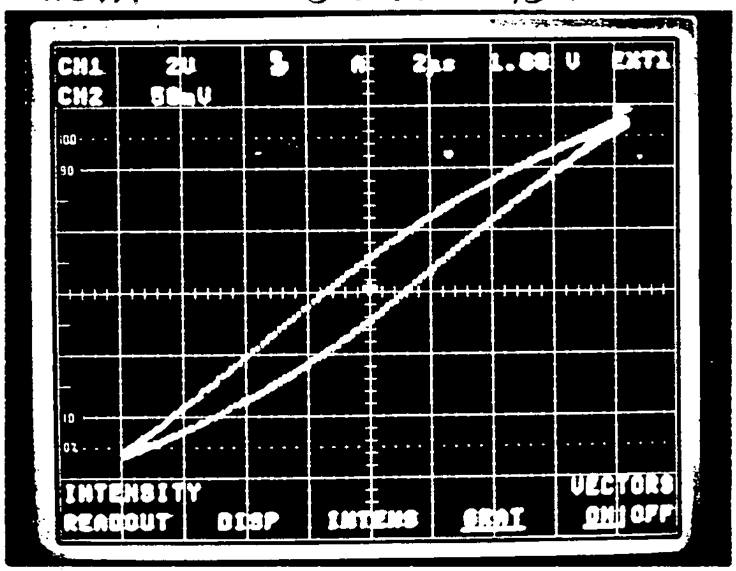
Size	FLAT Location 1	CENTER Location 2	TOP Location 3
Vt (volts)	-1.01	-.963	leaky (doesn't shut off no V_T)
Beta (uA/V²)	14.0	13.9	13.4

Contact Strings:

Size	FlAT Location 1	center Location 2	top Location 3	
Al-Tel ~~Kohms~~	49.6Ω	53.25Ω	47.9Ω	
Al-N+ Kohms	2.170	2.20	2.20	
Al-P+ Kohms	22.7 ξ	20.0	13.9	@ 5V

resistance decreasing as increase voltage

7139A ECD 512 0/50/50

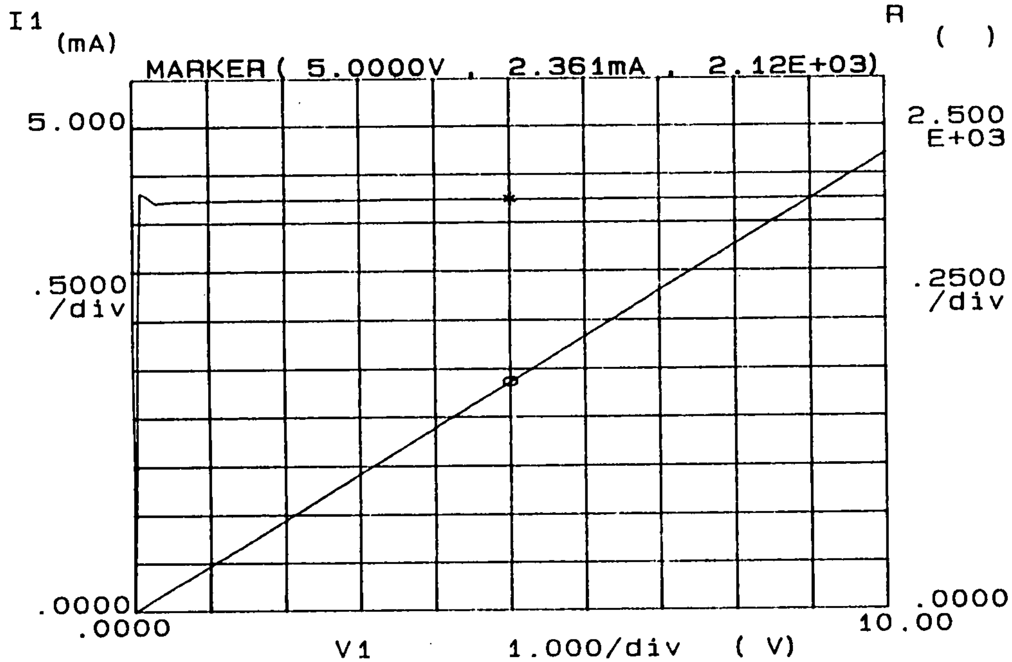


May 26, 1987

0/50/50 material 5-6 $\mu C/cm^2$, for material that has not been stressed it is slim looped for 0/50/50.

****** GRAPHICS PLOT ******

ECD512A 7193A 0/50/50 AL-N+



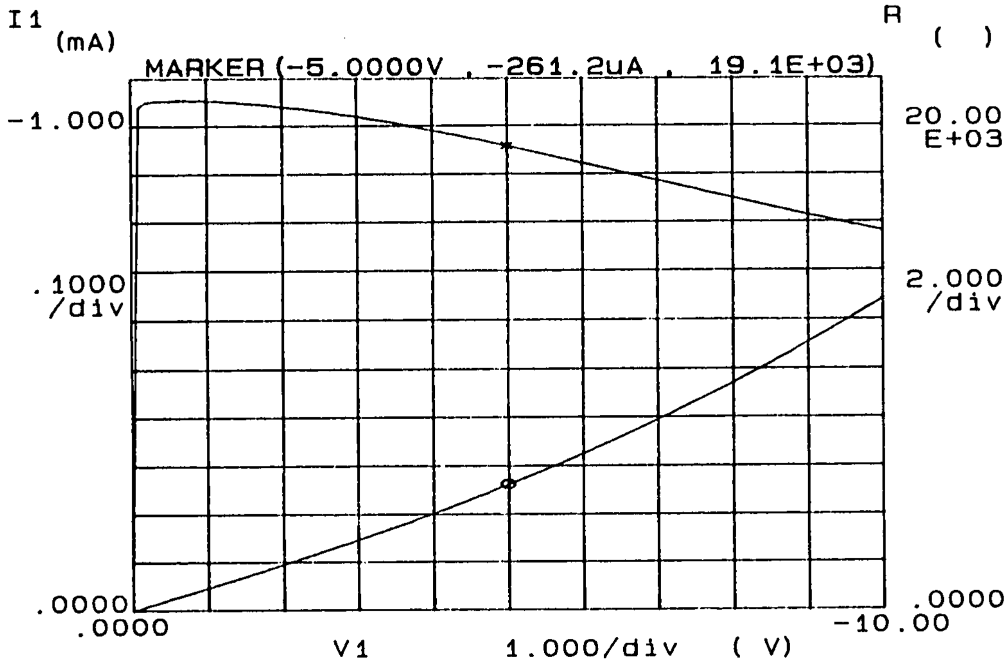
Variable1:
V1 -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V2 -Ch2 .0000V
V3 -Ch3 .0000V
V4 -Ch4 .0000V

R ( ) = V1/I1

****** GRAPHICS PLOT ******

ECD512A 7193A 0/50/50 AL-P+



Variable1:
V1 -Ch1
Linear sweep
Start .0000V
Stop -10.000V
Step - .1000V

Constants:
V2 -Ch2 .0000V
V3 -Ch3 .0000V
V4 -Ch4 .0000V

R ( ) = V1/I1

Krysalis Confidential

Parametric Data

Date : June 1, 1987

Foundry : Orbit

Wafer ID: 7148A (8/40/60)

Wafer Description: ECD 512A

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Transistor Parametrics

N-ch:

Size	Flat Location 1	Center Location 2	Top Location 3
Vt (volts)	.790	.718	.867
Beta (uA/V²)	42.4	41.2	40.0

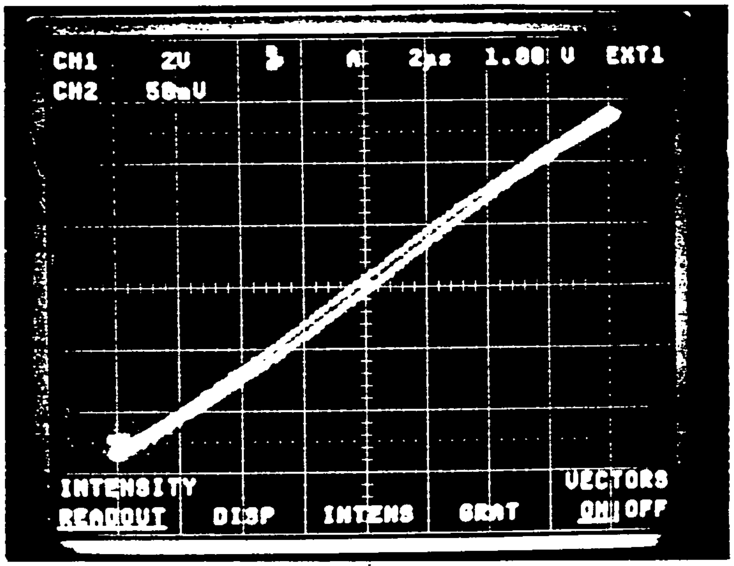
P-ch:

Size	Flat Location 1	Center Location 2	Top Location 3
Vt (volts)	-.875	-.837	-.738
Beta (uA/V²)	14.6	15.1	13.8

Contact Strings:

Size	Flat Location 1	center Location 2	top Location 3
Al-Tel Ω ~~Kohms~~	501 Ω	501 Ω	501 Ω
Al-N+ Kohms	1.73	1.77	1.77
Al-P+ Kohms	6130	2700	~~7.096 x~~ 7096

ECD 512



7148 A 8/40/60 6-2-87

Slim looped ≈ 1-2 μC/cm²
Looked at five different spots on the wafers results the same. All ~~material~~ devices measured slim looped.

Krysalis Confidential

Parametric Data

Date : June 1, 1987

Foundry : Orbit

Wafer ID: ~~ECD512A~~ 7148 B

Wafer Description: 0/50/50 ECD512A

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Transistor Parametrics

N-ch:

Size	Location 1 (Flat)	Location 2 (Center)	Location 3 (Top)
Vt (volts)	.804	.821	.868
Beta (uA/V²)	42.4	42.5	41.9

P-ch:

Size	Location 1 (Flat ~~Top~~)	Location 2 (Center)	Location 3 (top)
Vt (volts)	-.891	-.875	-.717
Beta (uA/V²)	14.0	14.6	14.8

Contact Strings:

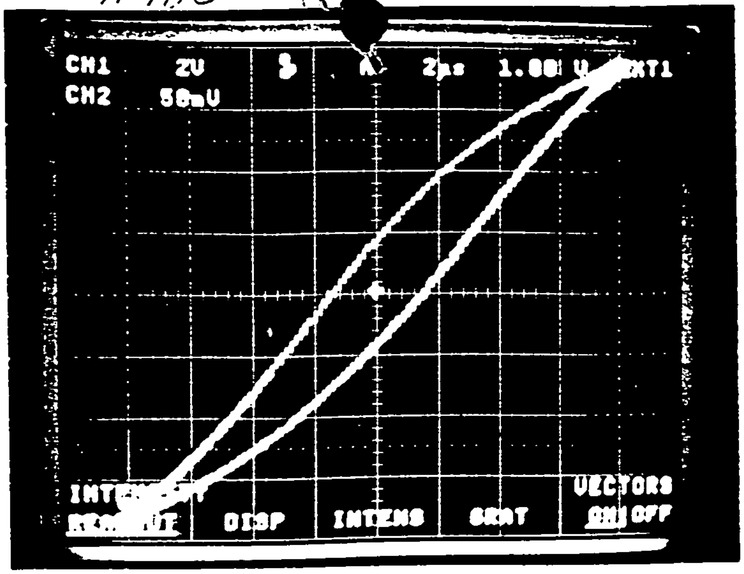
Size	Location 1 (Flat)	Location 2 (Center)	Location 3 (top)
Al-Tel ~~Kohms~~	40 Ω	31.9 Ω	39.1 Ω
Al-N+ Kohms	1.73 KΩ	1.83 KΩ	1.78 KΩ
Al-P+ Kohms	283 KΩ	707 KΩ	186 KΩ

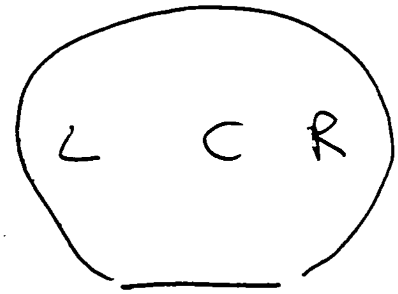
@ 5V

7148B 6-2-87

8-9 $\mu C/cm^2 \cong \Delta P$

Left



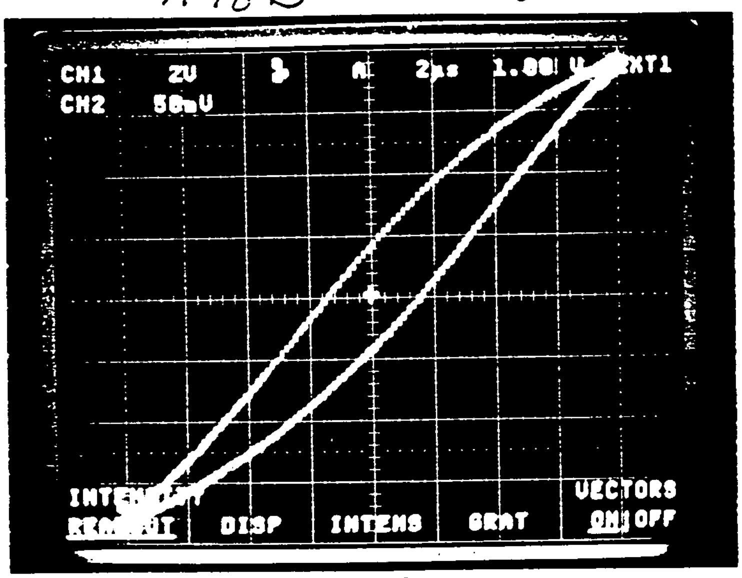


01

7148B 6-2-87

8-9 $\mu C/cm^2 \cong \Delta P$

Center

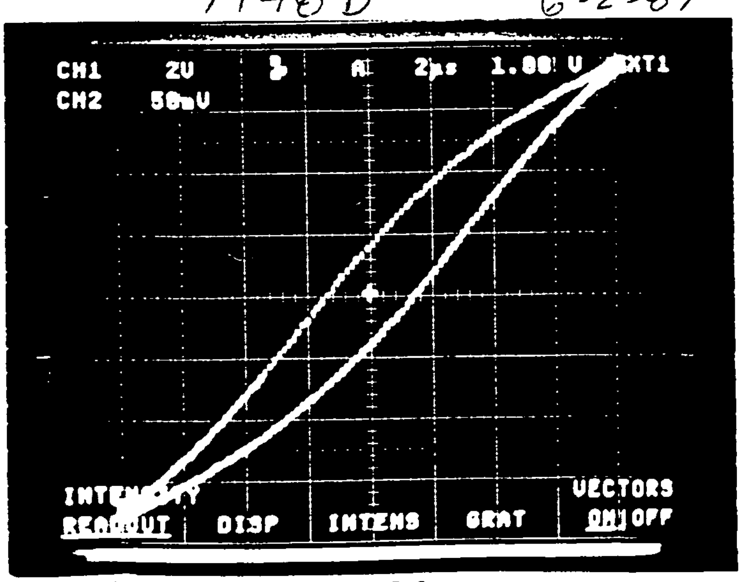


0/50/50 ECD 512A

7148B 6-2-87

8-9 $\mu C/cm^2 \cong \Delta P$

Right



0/50/50 ECD 512A